



# SKM-U

Rev : 1.1

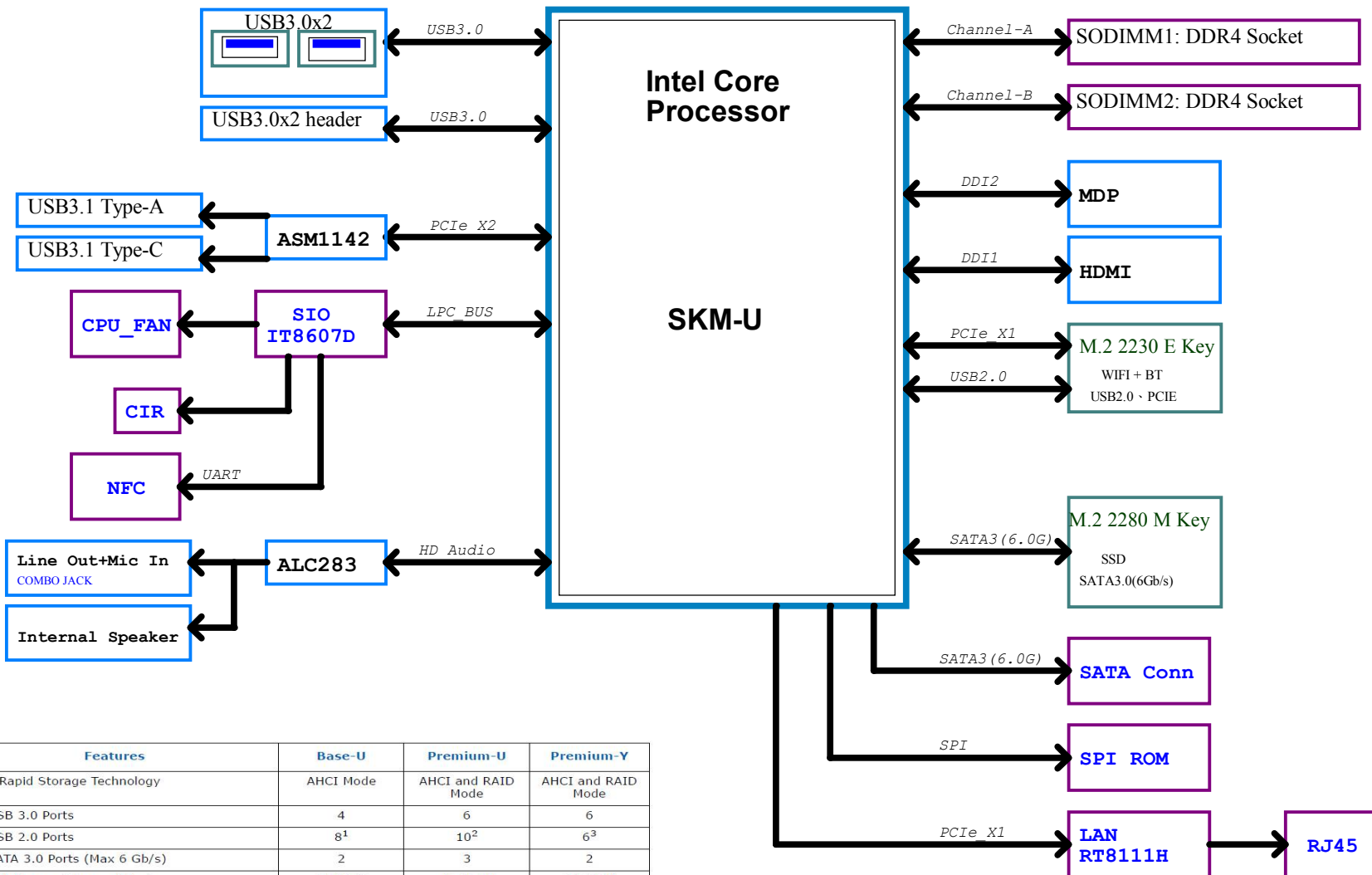
TABLE OF CONTENTS

Page	Index	Page	Index
1	Cover Page	26	DC-IMVP8-VCCGT
2	Block Diagram	27	DC-IMVP8 -VCCGTX
3		28	DC-IMVP8-VCCSA
4	CPU-MISC/DDI	29	+VDDQ/+DDR_VPP
5	CPU-DDR3-CHA	30	SYS_POWER
6	CPU-DDR3-CHB	31	+PS5VSB/+PS3VSB
7	CPU-PE/USB/GPIO	32	+V1P8A/+VCCIO
8	CPU-SATA/CLOCK/RTC	33	+V1P0A
9	CPU-SPI/LPC/SMB	34	DC-VCC/VCC3/DC_VIN
10	CPU-CFG/LPC_DEBUG	35	USB3.1 TypeC
11	CPU-PWR-1	36	USB3.1 IC
12	CPU-PWR-2	37	USB3.1 Type-A
13	CPU-GND	38	104/STRAPPING
14	SO-DIMM	39	GPIO Function
15	SATA_PWR/SATA CONN/BIOS_SEC	40	Power Sequence
16	USB3.0/USB2.0	41	POWER DELIVERY
17	NFC/WC/LOGO		
18	AUDIO-ALC283		
19	SIO-IT8607		
20	LAN RT8111H-CG		
21	M.2 2280/2230		
22	Mini-DP		
23	HDMI/LEVEL SHIFTER		
24	FAN/BTN/PWR LED		
25	DC-IMVP8-VCORE		

REVISION HISTORY:

Rev	Date	Notes
-----	------	-------





Features	Base-U	Premium-U	Premium-Y
Intel® Rapid Storage Technology	AHCI Mode	AHCI and RAID Mode	AHCI and RAID Mode
Total USB 3.0 Ports	4	6	6
Total USB 2.0 Ports	8 <sup>1</sup>	10 <sup>2</sup>	6 <sup>3</sup>
Total SATA 3.0 Ports (Max 6 Gb/s)	2	3	2
Total PCI Express* Lanes (Gen)	10 (2.0)	12 (3.0)	10 (3.0)
Total Intel® RST capable PCIe and SATA Express <sup>4</sup> Storage Devices	0	2 <sup>5</sup>	2 <sup>5</sup>

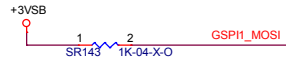
Features	Base-U	Premium-U	Premium-Y
<b>Notes:</b> 1. USB 2.0 port numbers: 1-8 2. USB 2.0 port numbers: 1-10 3. USB 2.0 port numbers: 1-6 4. SATA Express Capable Ports (x2) 5. Intel® RST PCIe supports RAID configuration 0/1			

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A



HDMI

mDP



Boot Device Select:

BOOT DEVICE	GSPI1_MOSI
SPI	0
LPC	1

GSPI1\_MOSI internal pull-down

Strap Pin Select:

Strap Pin	GPP_B18
No Reboot (DI)	0
No Reboot (EN)	1

GPP\_B18 internal pull-down

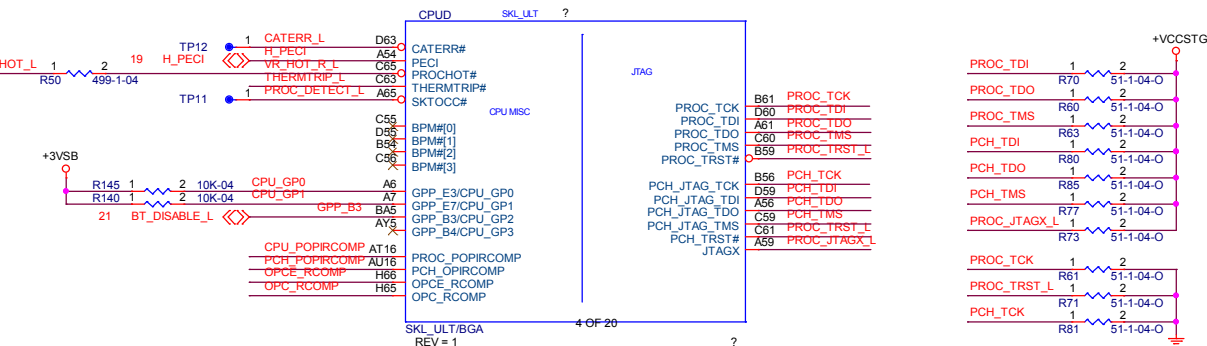
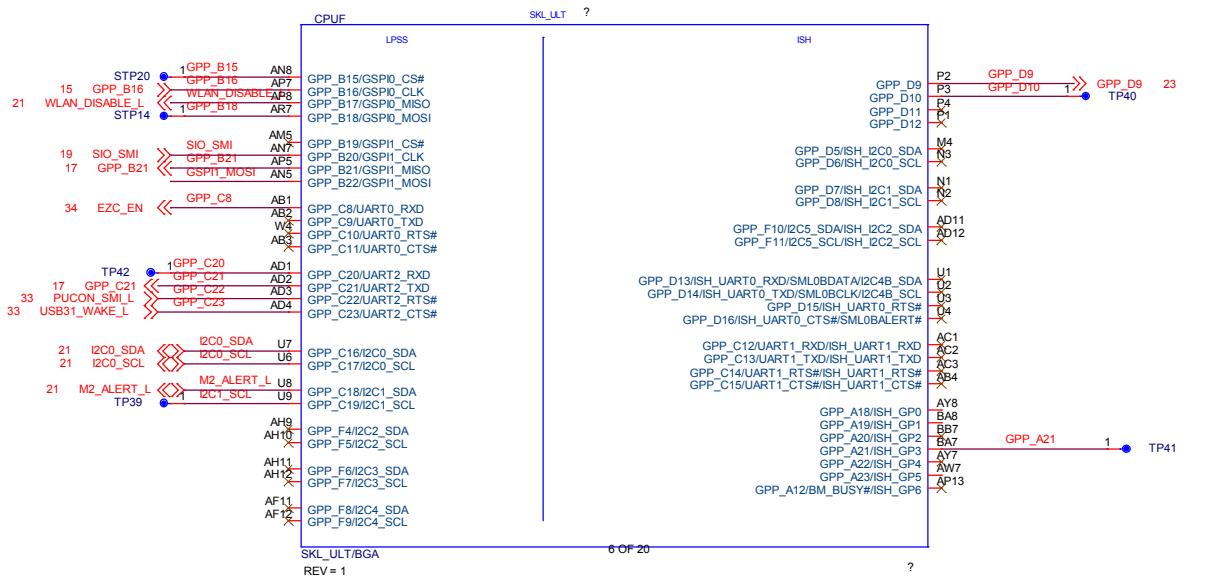
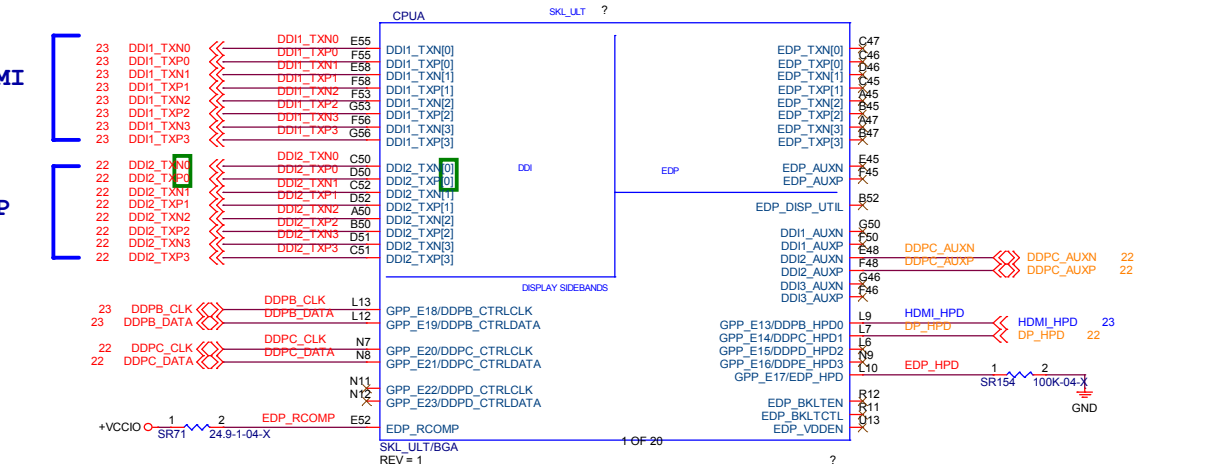
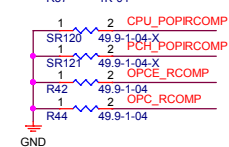
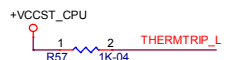
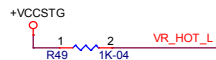
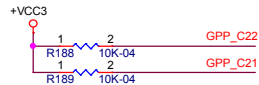
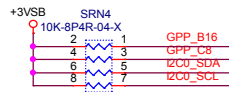
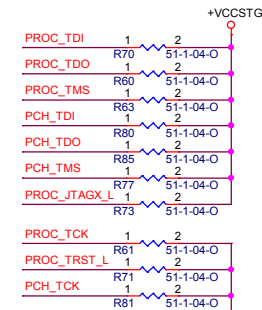
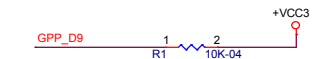


Table 7-1. Mapping of HDMI\* Signals for DDI Ports

Port	Digital Display Interface Plus	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMI1_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMI1_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMI1_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMI1_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMI1_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMI1_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMI1_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMI1_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK
Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMI2_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMI2_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMI2_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMI2_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMI2_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMI2_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMI2_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMI2_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CLK



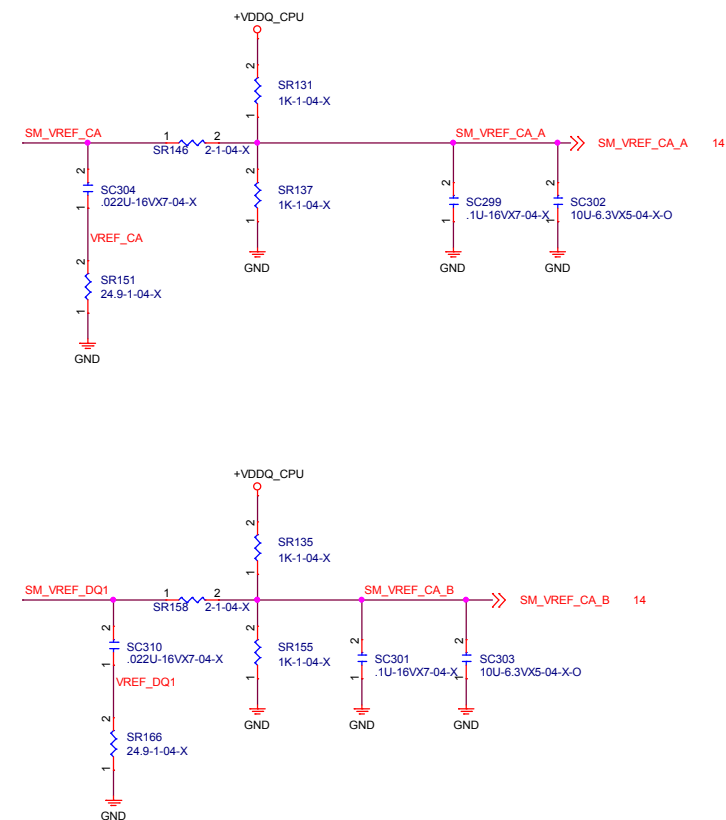
**Elitegroup Computer Systems**

Title: **CPU-MISC/DDI**

Size: Document Number **SKM-U** Rev **1.1**

Date: Tuesday, March 28, 2017 Sheet 4 of 38











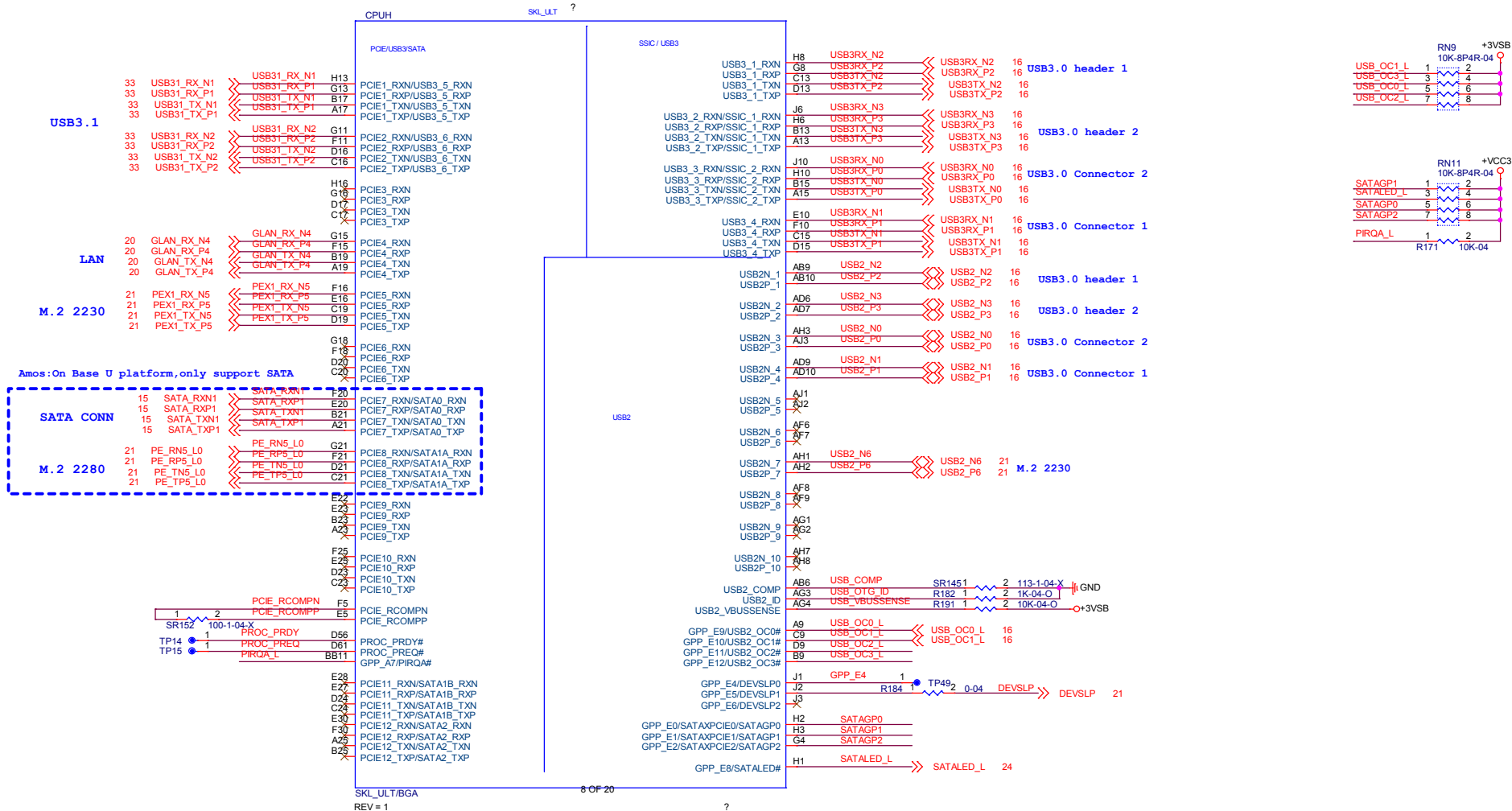
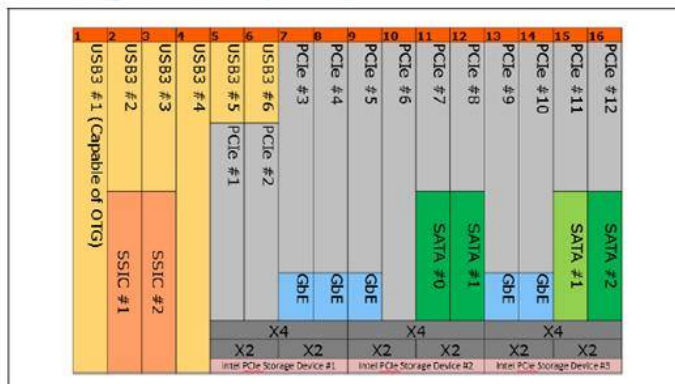
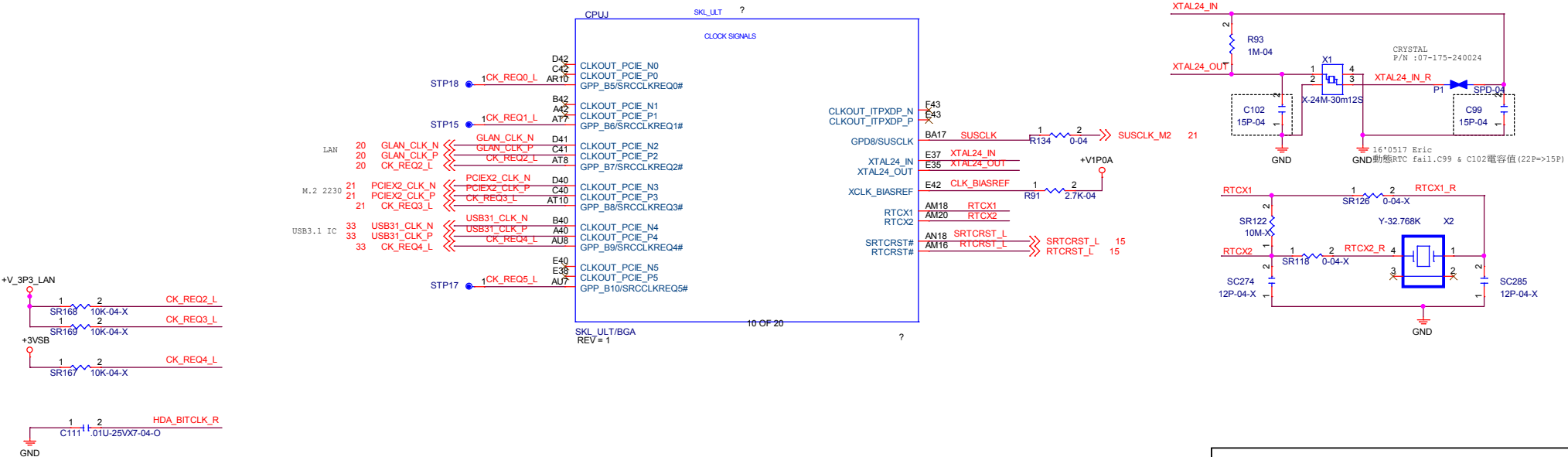


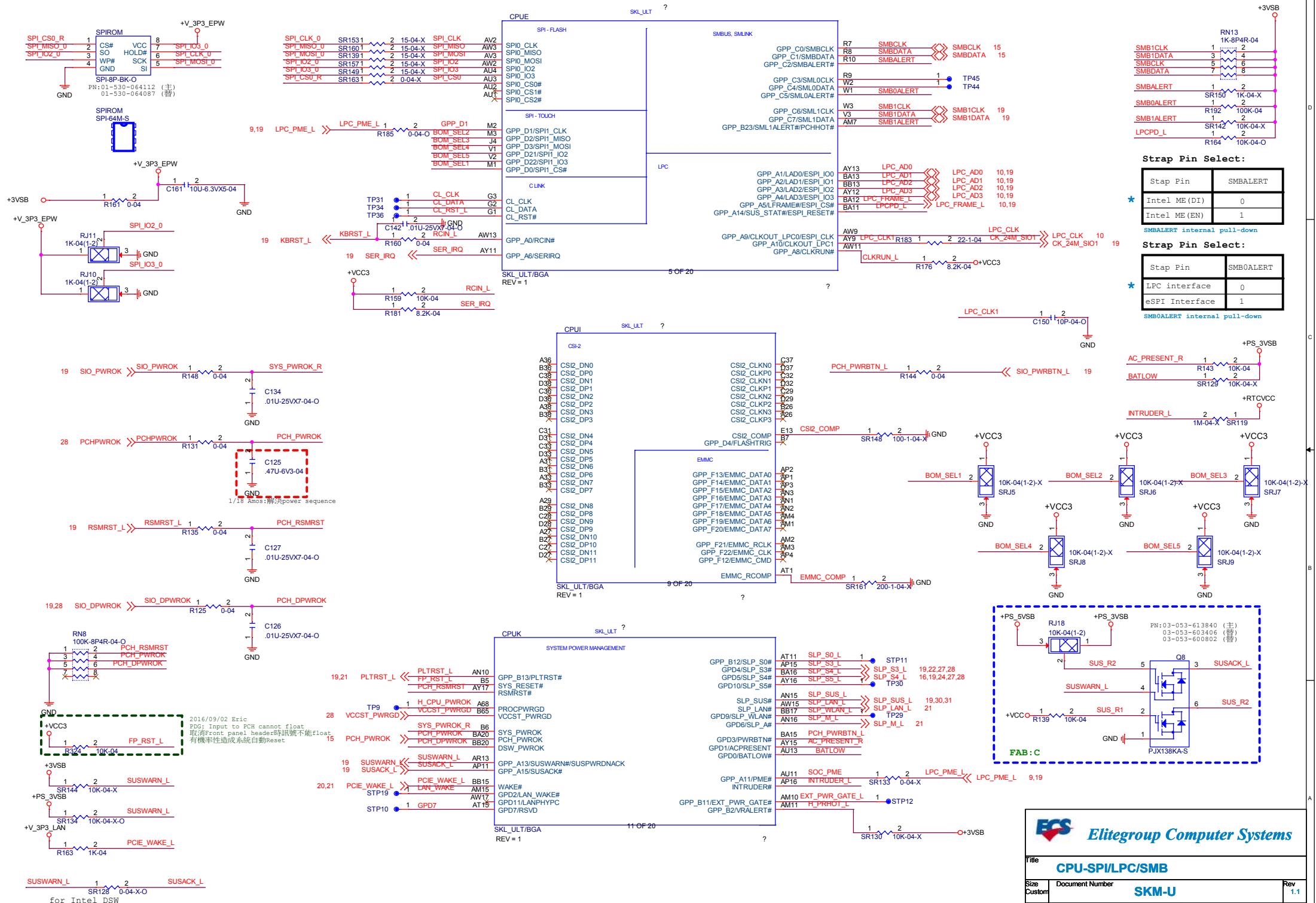
Figure 3-1. HSI0 Muxing on SKL PCH-LP (U Series)











**Strap Pin Select:**

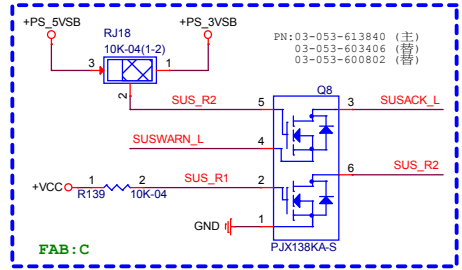
Strap Pin	SMBALERT
Intel ME (DI)	0
Intel ME (EN)	1

*SMBALERT internal pull-down*

**Strap Pin Select:**

Strap Pin	SMB0ALERT
LPC interface	0
eSPI Interface	1

*SMB0ALERT internal pull-down*



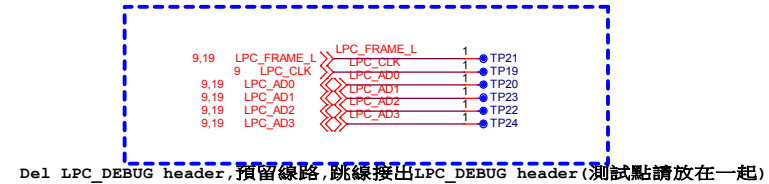
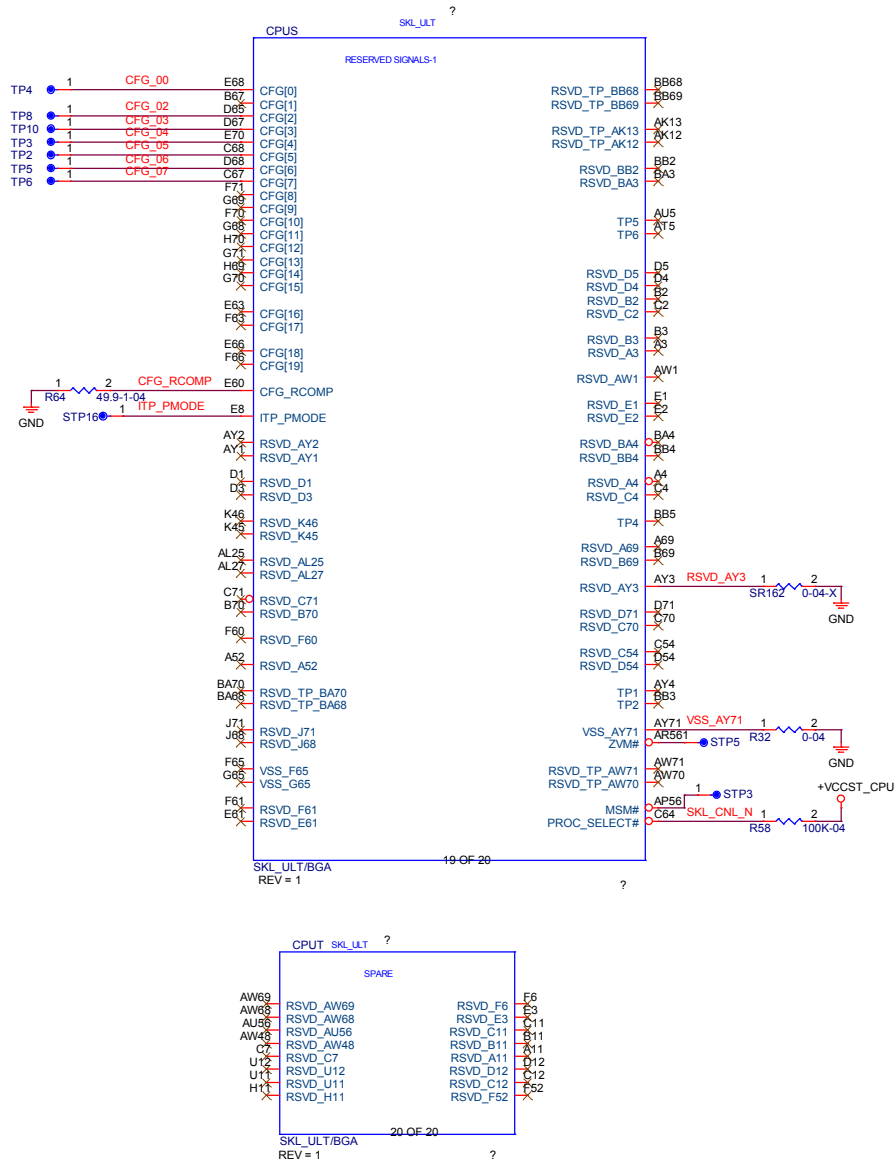
**CPU-SPI/LPC/SMB**

Document Number **SKM-U**

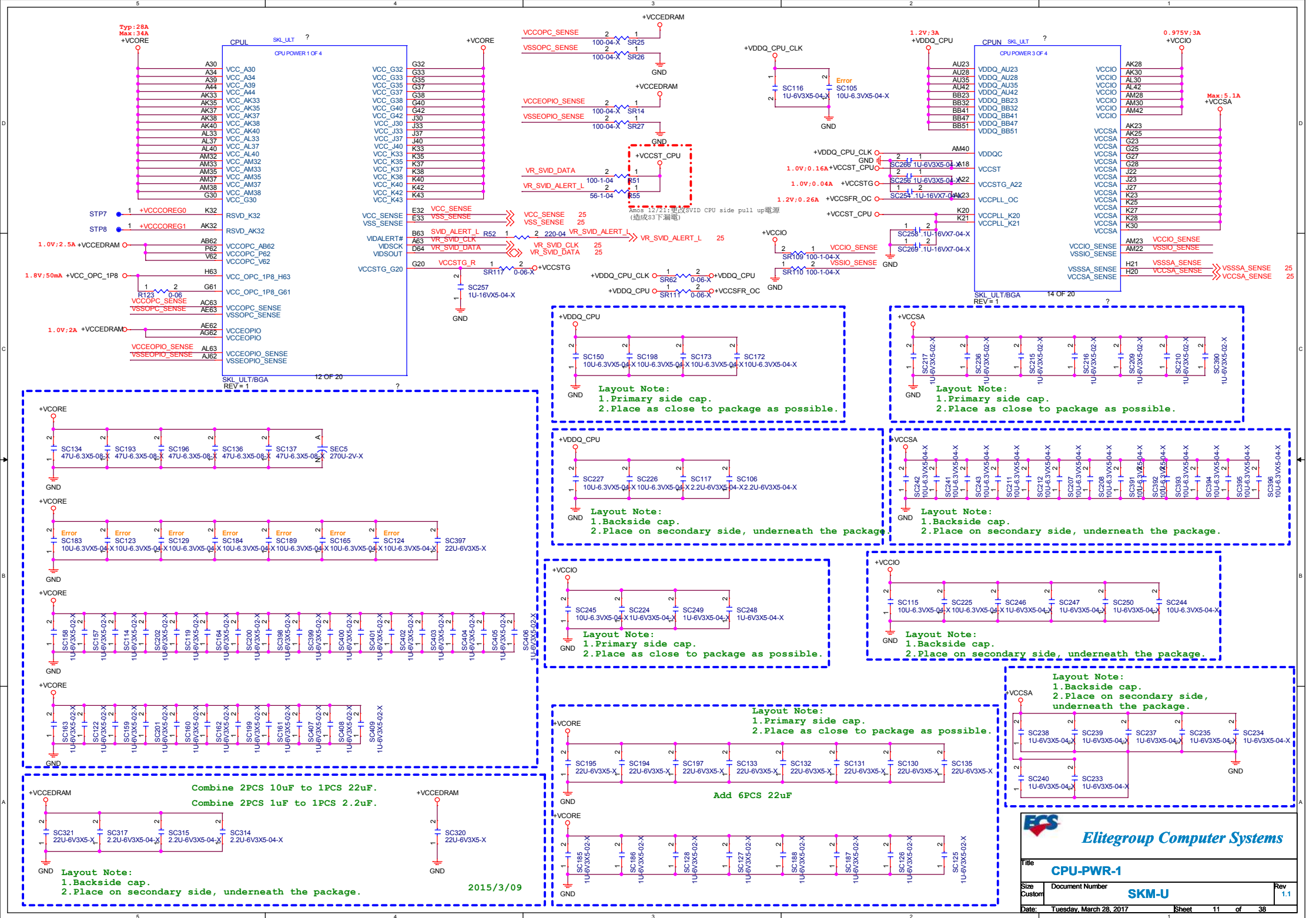
Date: Tuesday, March 28, 2017 Sheet 9 of 38

2016/09/02 Eric  
PDG: Input to PCH cannot float  
取消front panel header時訊號不能float  
有機率性造成系統自動Reset





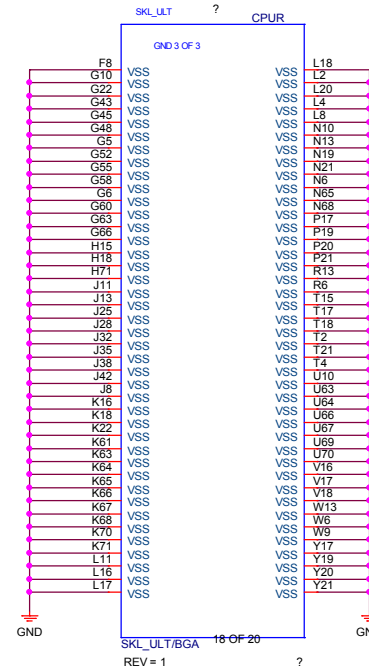
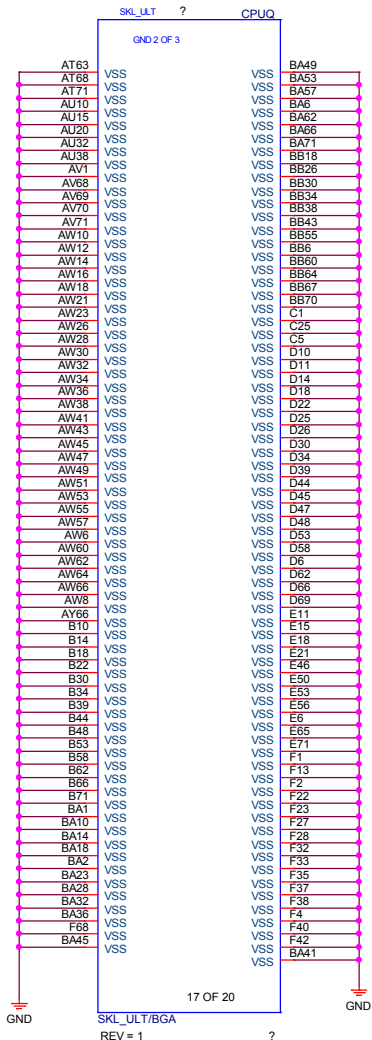
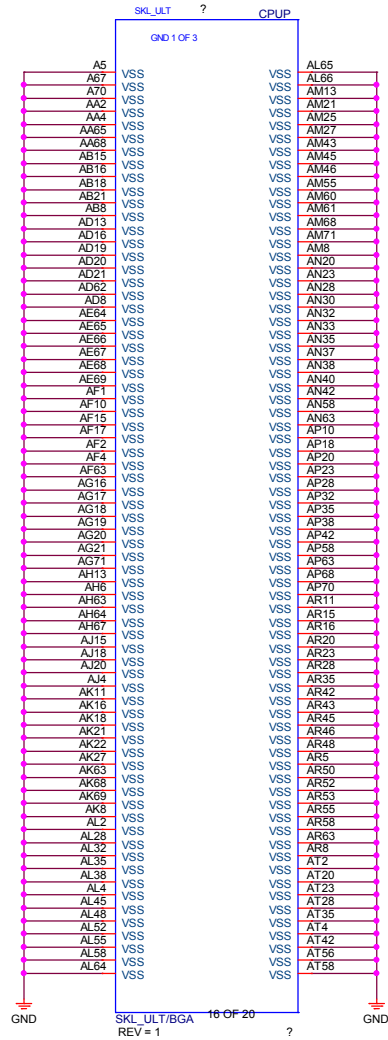




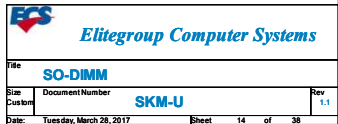




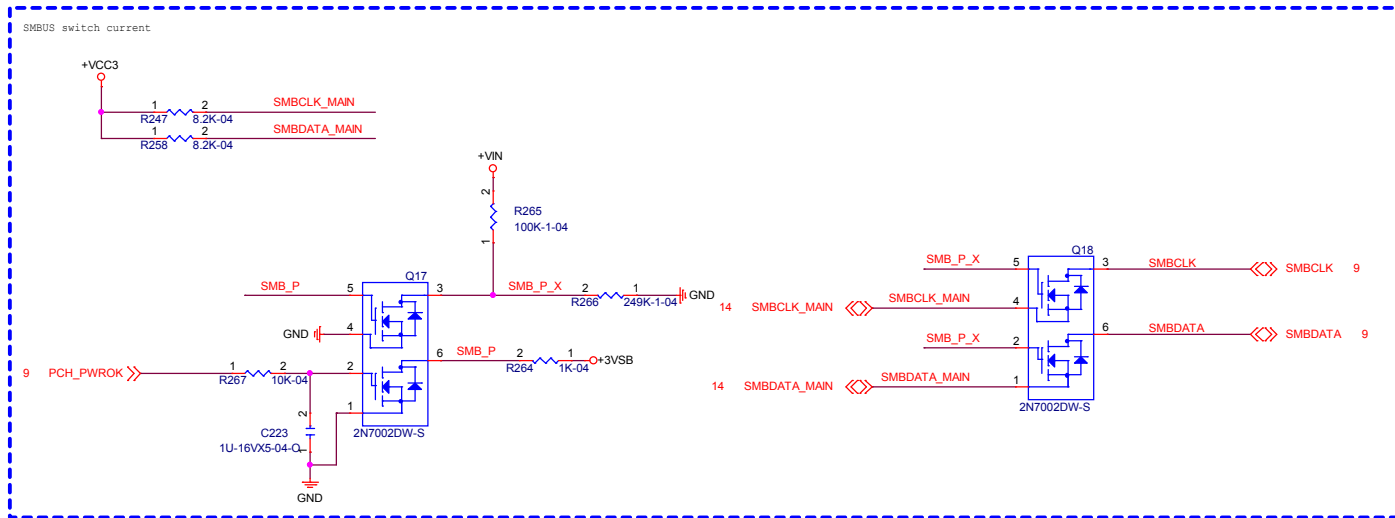




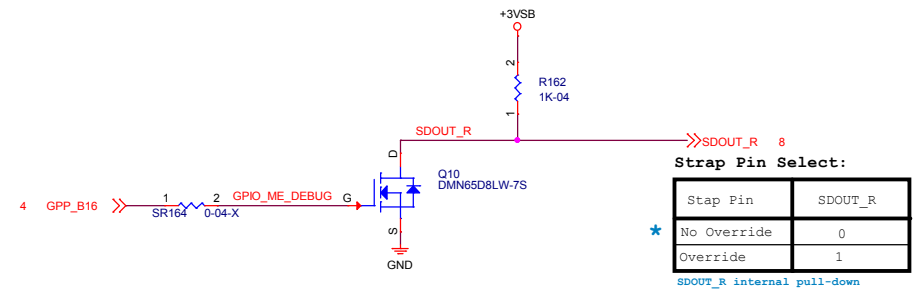
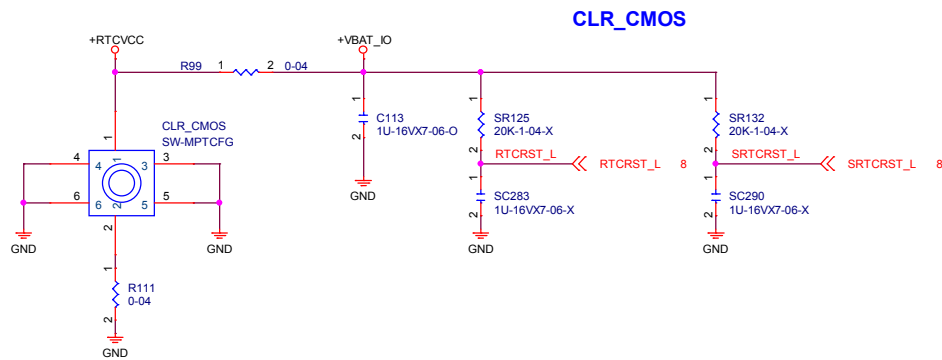
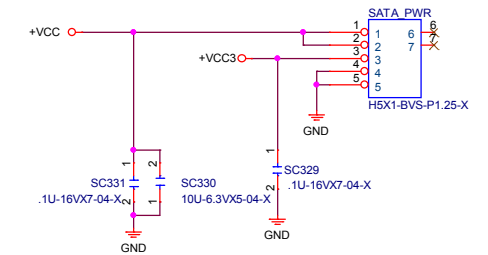
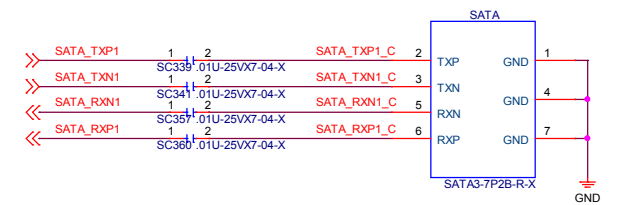






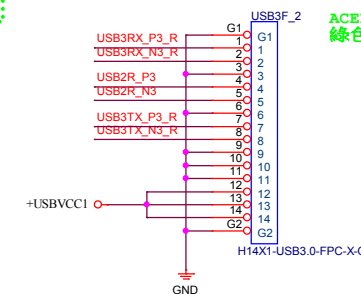
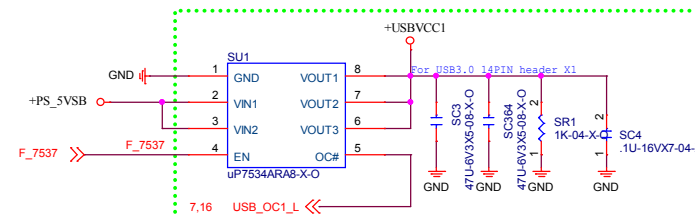
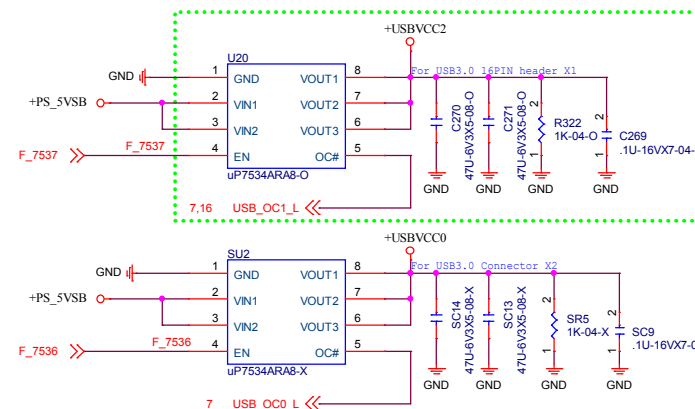
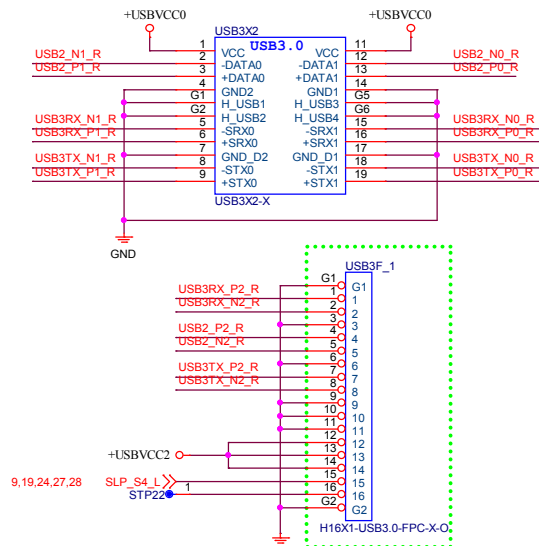
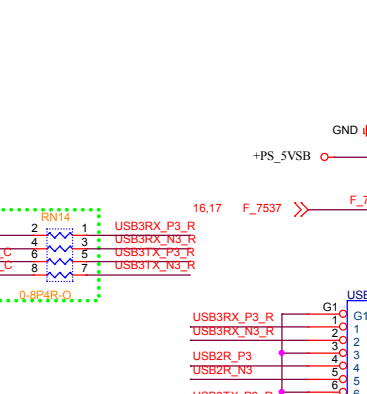
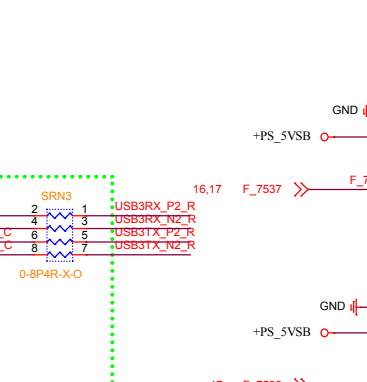
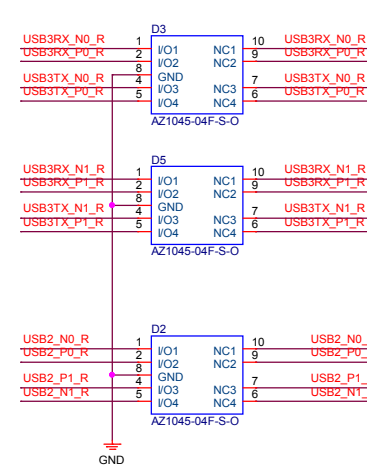
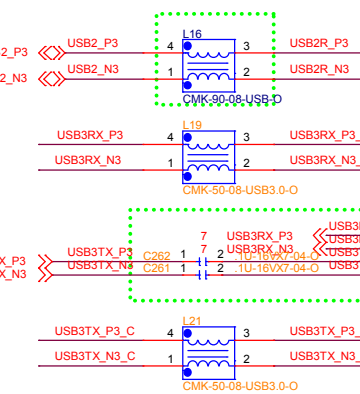
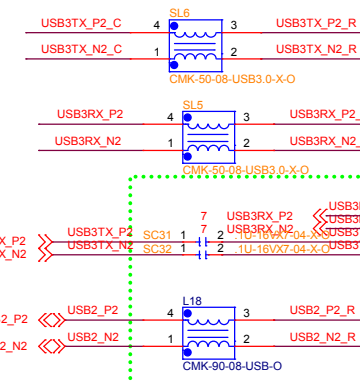
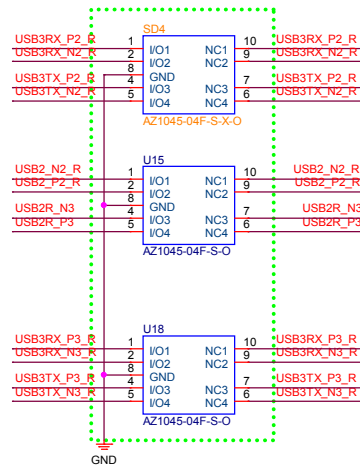
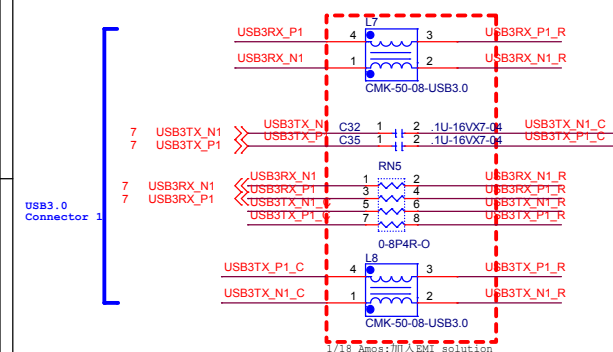
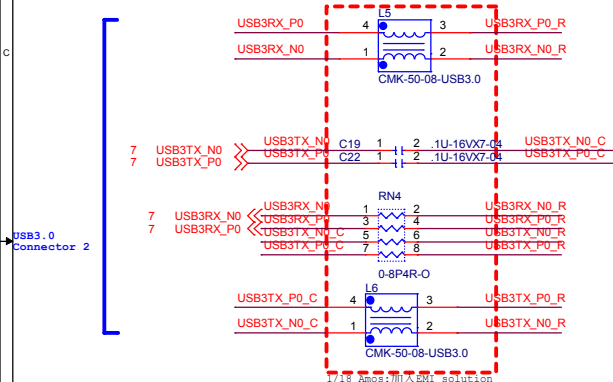
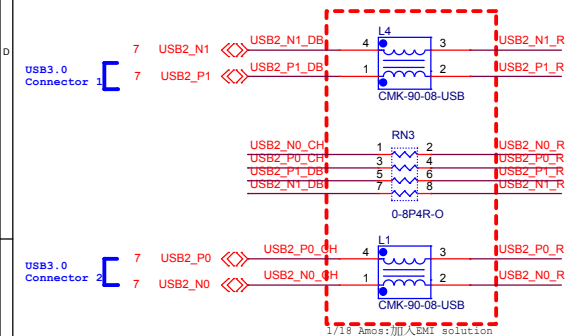


7 SATA\_TXP1  
7 SATA\_TXN1  
7 SATA\_RXN1  
7 SATA\_RXP1





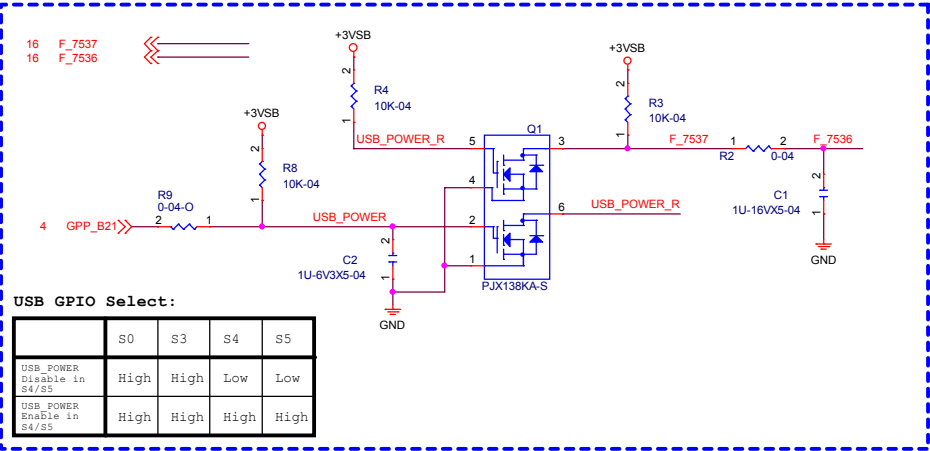
## USB3.0 Connector



20150805 Amos:Del USB Charging current



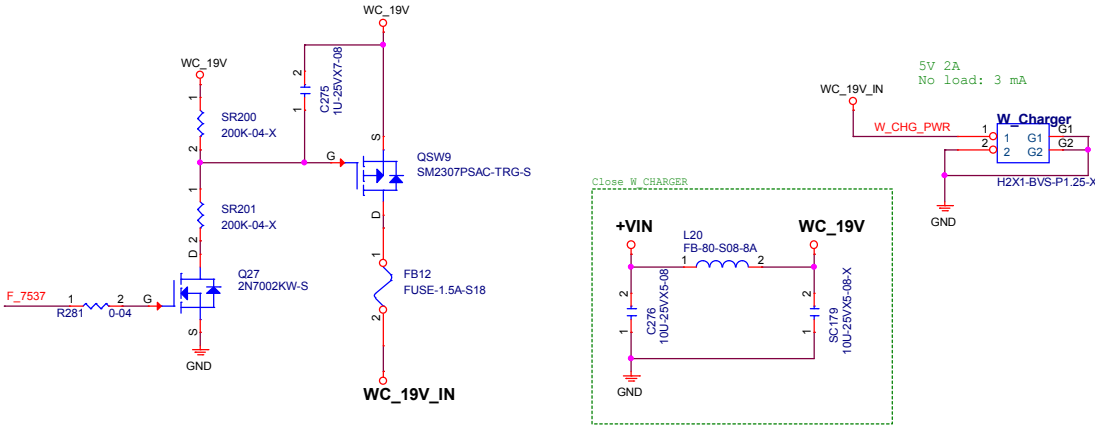
USB 3.0 & 2.0 power Enable current



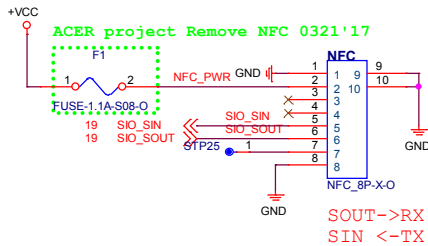
USB GPIO Select:

	S0	S3	S4	S5
USB_POWER Disable in S4/S5	High	High	Low	Low
USB_POWER Enable in S4/S5	High	High	High	High

Wireless charging header



NFC header



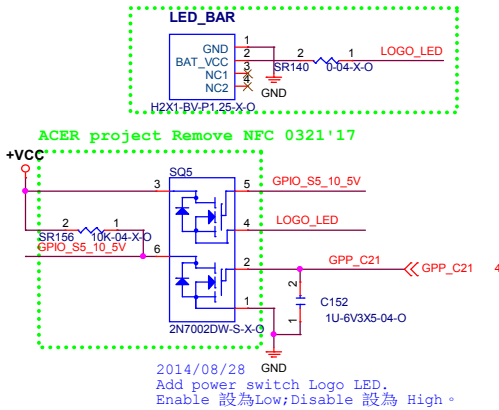
NFC card PIN define

Cable PIN define:  
Card/Header  
1=>8 2=>7 3=>6  
4=>5 5=>4 6=>3  
7=>2 8=>1

2. Interface Connector

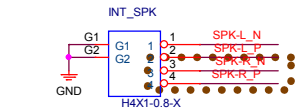
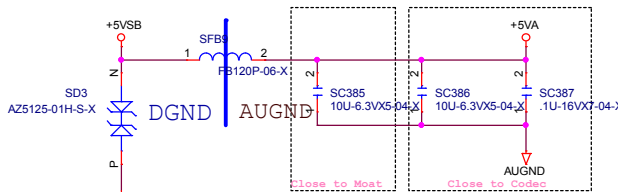
Pin Number	Definition	Description
1	GND	GND
2	RF	RF
3	TX	UART TXD
4	Rx	UART RXD
5	NC	NC
6	NC	NC
7	Vcc	Input VV
8	GND	GND

LOGO LED header



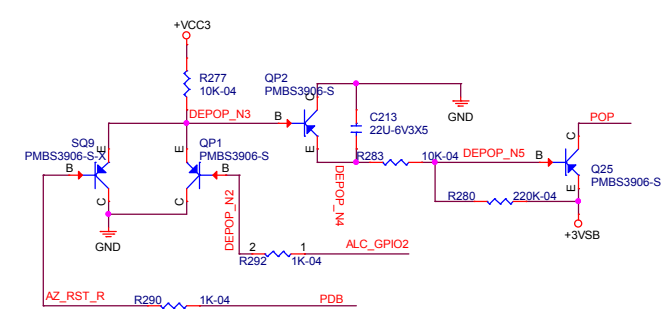
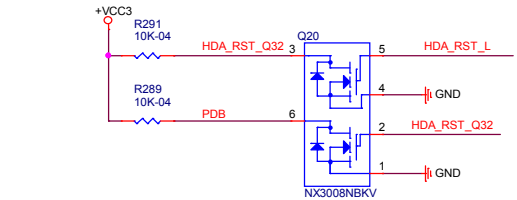
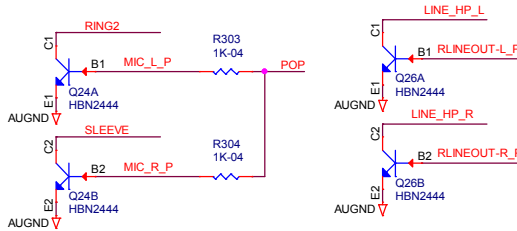
20150805 Amos:Del auxiliary Power connector



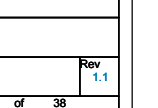
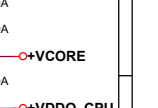
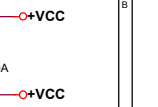
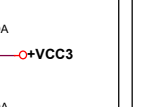
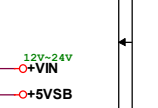
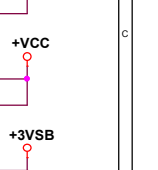
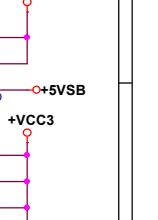
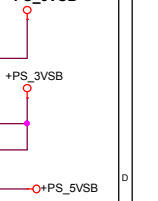
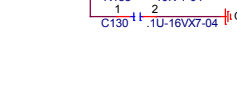
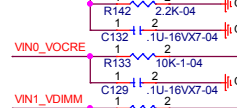
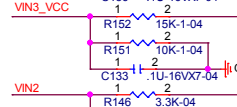
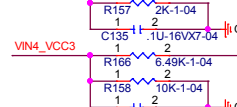
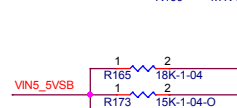
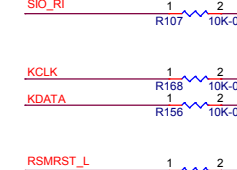
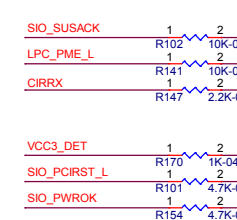
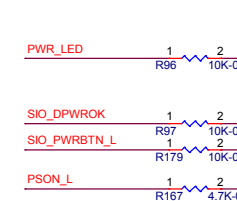
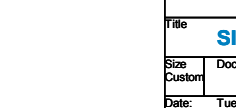
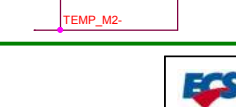
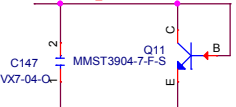
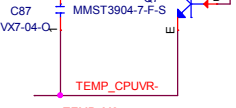
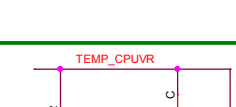
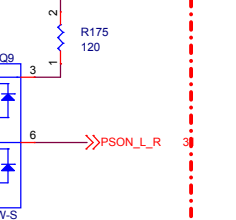
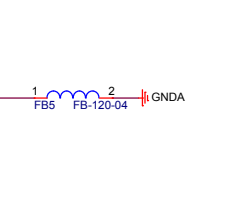
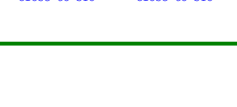
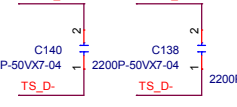
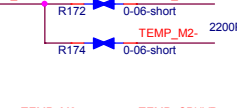
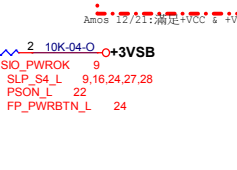
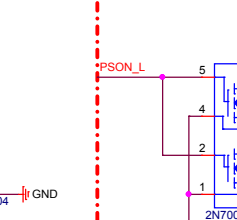
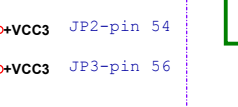
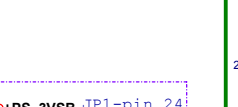
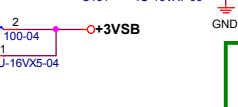
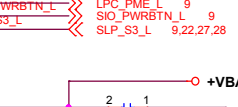
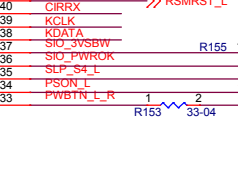
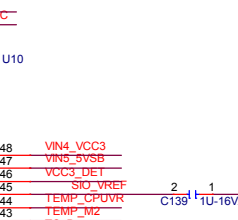
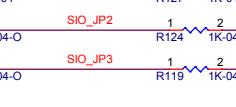
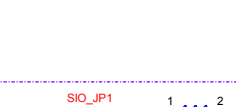
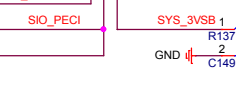
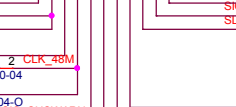
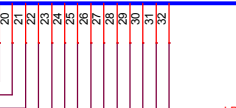
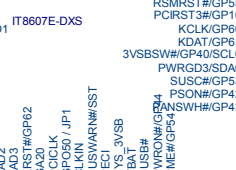
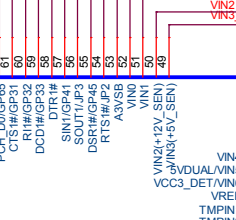
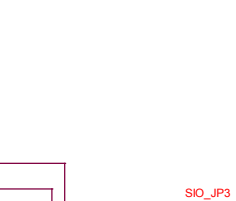
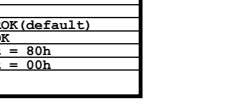
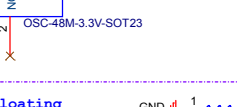
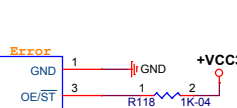
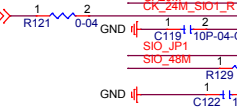
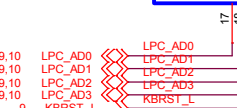
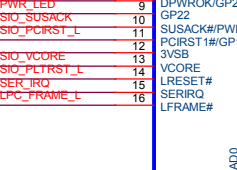
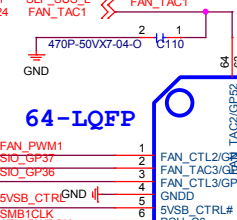
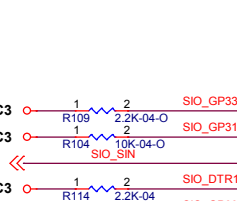
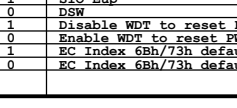
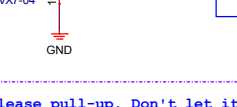
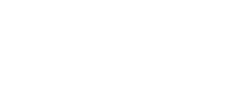
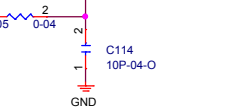
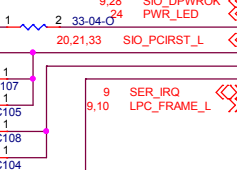
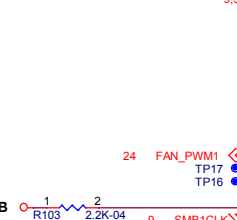
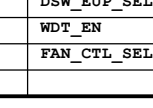
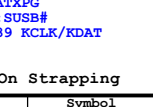
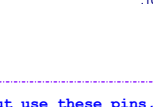
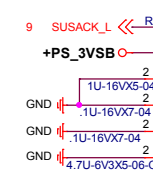
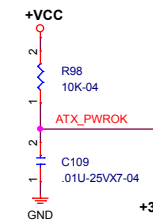
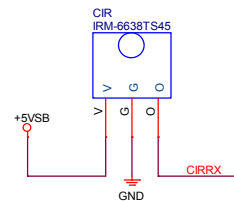


2015/05/04 注意  
ALC283 零件圖P1244、45定義與datasheet相反  
SPEAKER Connectors Pin 3、4正確定義:  
Pin3 SPK-R\_N ->SPK-R\_P  
Pin3 SPK-R\_P ->SPK-R\_N  
PM不動板端線路，所以請SPEAKER廠商在Connector接Pin3、4互換。

Speaker trace layout  
4 ohm : 40mil  
8 ohm : 20mil



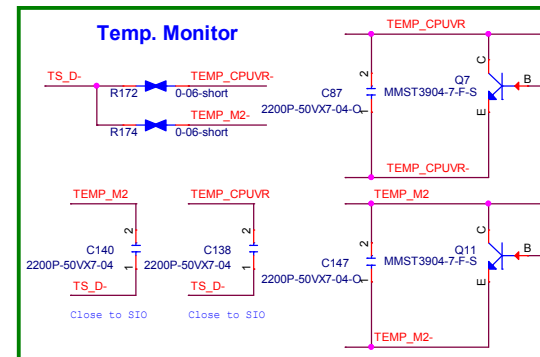




If without use these pins, Please pull-up. Don't let it floating  
 1.Pin 6:ATXPG  
 2.Pin 30:SUSB#  
 3.Pin38-39 KCLK/KDATA

# Power-On Strapping

Symbol	Value	Description
JP1	DSW_EUP_SEL	SIO_Eup
Pin-23	DSW	DSW
JP2	WDT_EN	Disable WDT to reset PWROK(default)
Pin-54	WDT_EN	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	EC Index 6Bh/73h default = 80h
Pin-56	FAN_CTL_SEL	EC Index 6Bh/73h default = 00h







LAN\_HSOP/N請接到SB的PCIE RX端

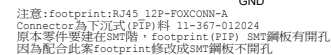
LAN HSIP/N在SB的PCIE TX端要記

LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

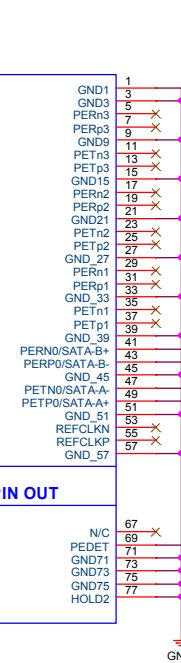
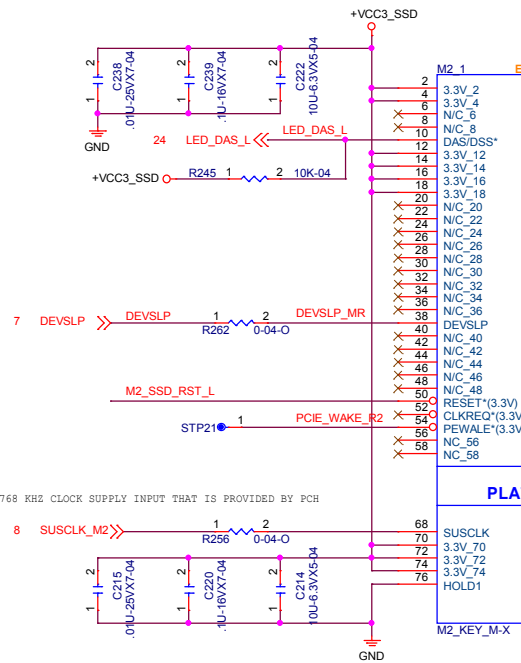
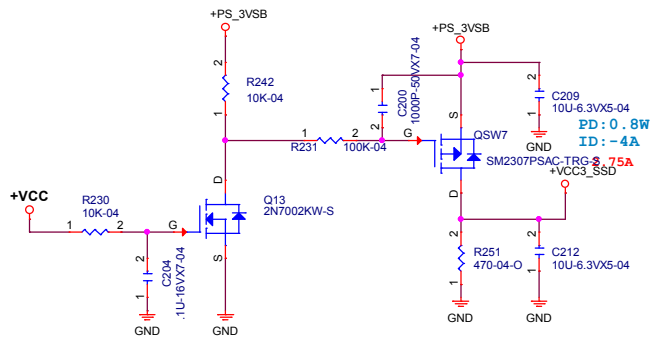
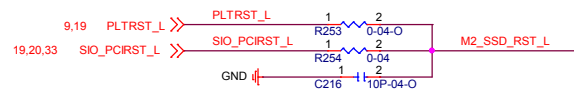


4

01-267-111367







**M key SATA: PIN 41 43 47 49**

PERN SATA RP SC377 1 2 01U-25VX7-04-X PE\_RP5\_L0 7

PERN SATA RN SC376 1 2 01U-25VX7-04-X PE\_RN5\_L0 7

PETN SATA TN SC374 1 2 01U-25VX7-04-X PE\_TN5\_L0 7

PETP SATA TP SC375 1 2 01U-25VX7-04-X PE\_TP5\_L0 7

**20150813 Amos: M.2 only support SATA.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

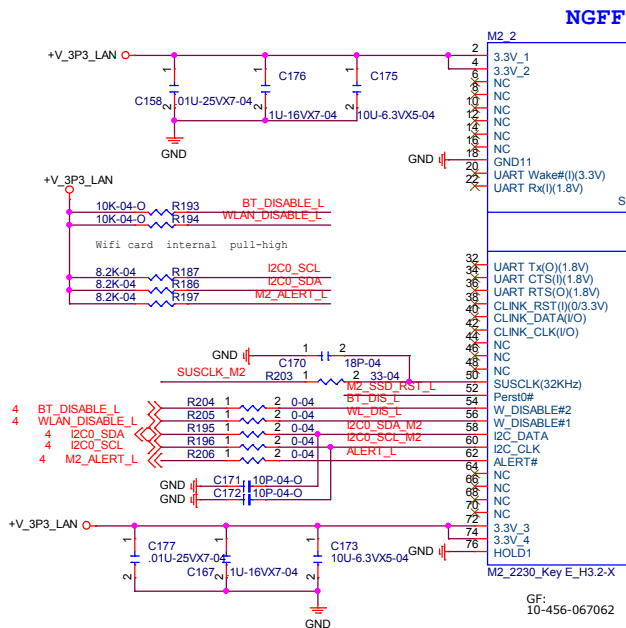
Pin	Signal	Pin	Signal
1	NC	41	PERN SATA RP
2	NC	42	PERN SATA RN
3	NC	43	PETN SATA TN
4	NC	44	PETP SATA TP
5	NC	45	NC
6	NC	46	NC
7	NC	47	NC
8	NC	48	NC
9	NC	49	NC
10	NC	50	NC
11	NC	51	NC
12	NC	52	NC
13	NC	53	NC
14	NC	54	NC
15	NC	55	NC
16	NC	56	NC
17	NC	57	NC
18	NC	58	NC
19	NC	59	NC
20	NC	60	NC
21	NC	61	NC
22	NC	62	NC
23	NC	63	NC
24	NC	64	NC
25	NC	65	NC
26	NC	66	NC
27	NC	67	NC
28	NC	68	NC
29	NC	69	NC
30	NC	70	NC
31	NC	71	NC
32	NC	72	NC
33	NC	73	NC
34	NC	74	NC
35	NC	75	NC
36	NC	76	NC
37	NC	77	NC
38	NC	78	NC
39	NC	79	NC
40	NC	80	NC
41	PERN SATA RP		
42	PERN SATA RN		
43	PETN SATA TN		
44	PETP SATA TP		
45	NC		
46	NC		
47	NC		
48	NC		
49	NC		
50	NC		
51	NC		
52	NC		
53	NC		
54	NC		
55	NC		
56	NC		
57	NC		
58	NC		
59	NC		
60	NC		
61	NC		
62	NC		
63	NC		
64	NC		
65	NC		
66	NC		
67	NC		
68	NC		
69	NC		
70	NC		
71	NC		
72	NC		
73	NC		
74	NC		
75	NC		
76	NC		
77	NC		
78	NC		
79	NC		
80	NC		

32.768 KHZ CLOCK SUPPLY INPUT THAT IS PROVIDED BY PCH

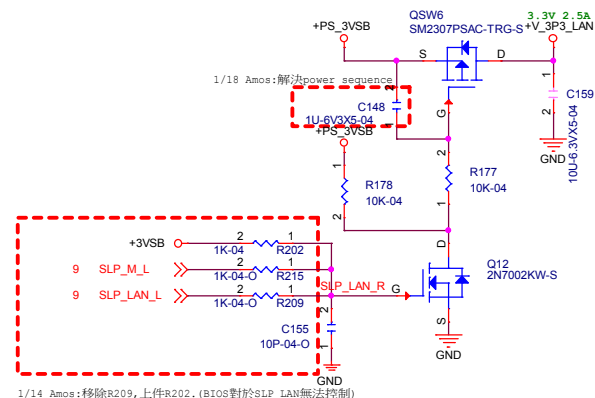
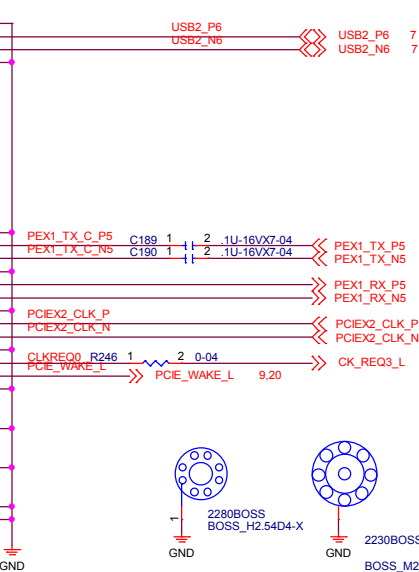
**KEY M PLATFORM PIN OUT**

M2\_KEY\_M-X

## LAN & M.2 2230 power switch



## NGFF

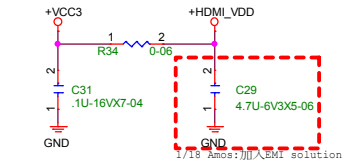
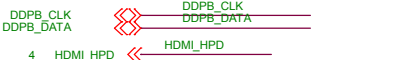
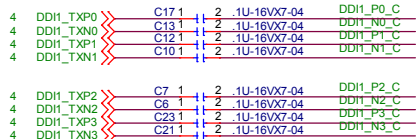


Title		M.2 2280/2230	
Size	Document Number	SKM-U	
Custom		Rev 1.1	
Date:	Tuesday, March 28, 2017	Sheet	21 of 38



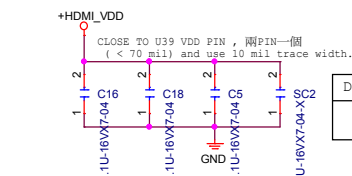




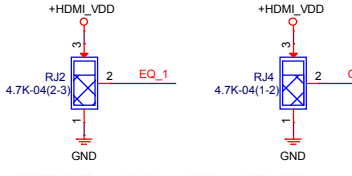
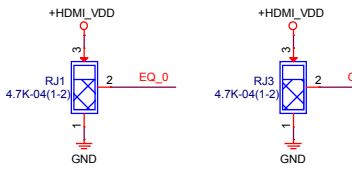


CLOSE TO R

CLOSE TO POWER PLANE TO 1442K



DDC_EN	Passgate
3.3V	Enable
	Disable

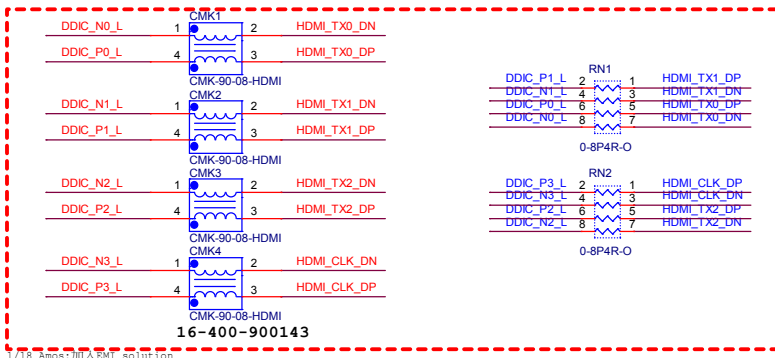


**TMDS Input Signal Equalization**

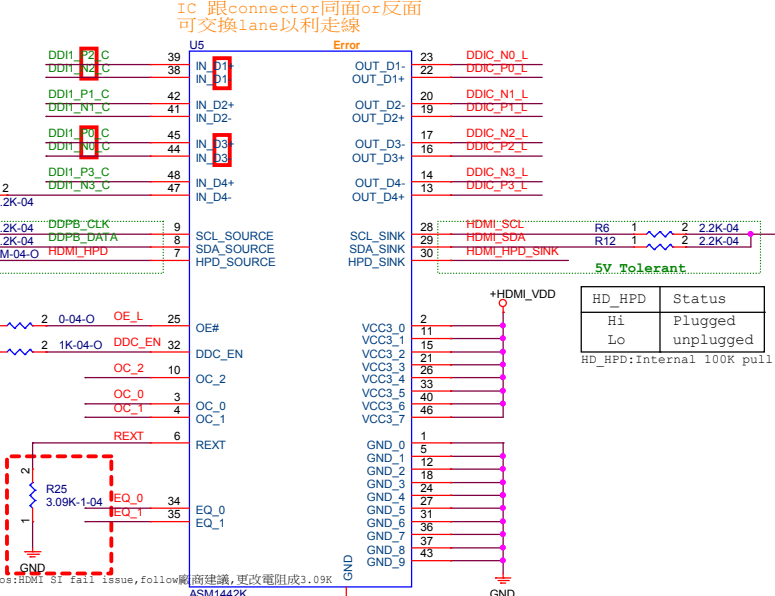
EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	3dB	
1	0	1dB	Default
1	1	0dB	

**TMDS Output Signal Integrity**

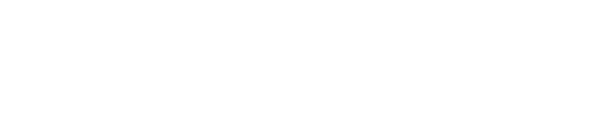
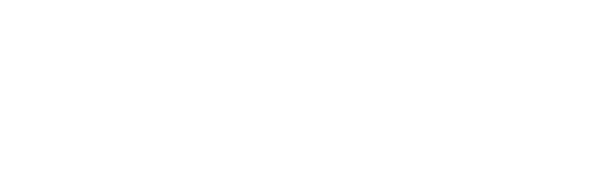
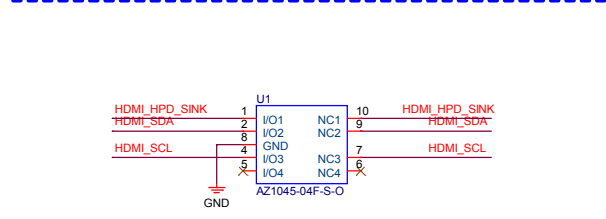
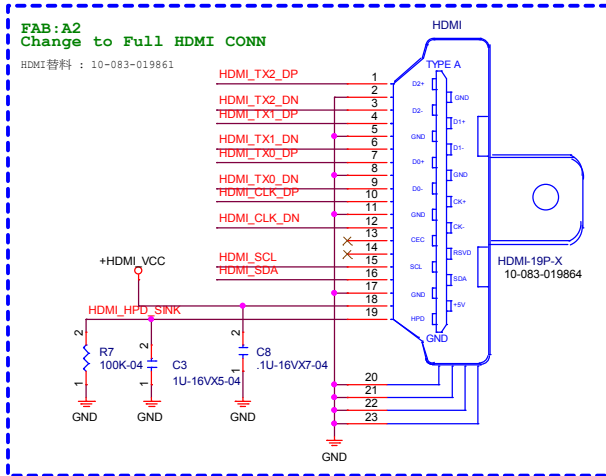
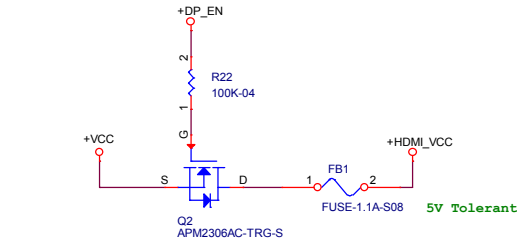
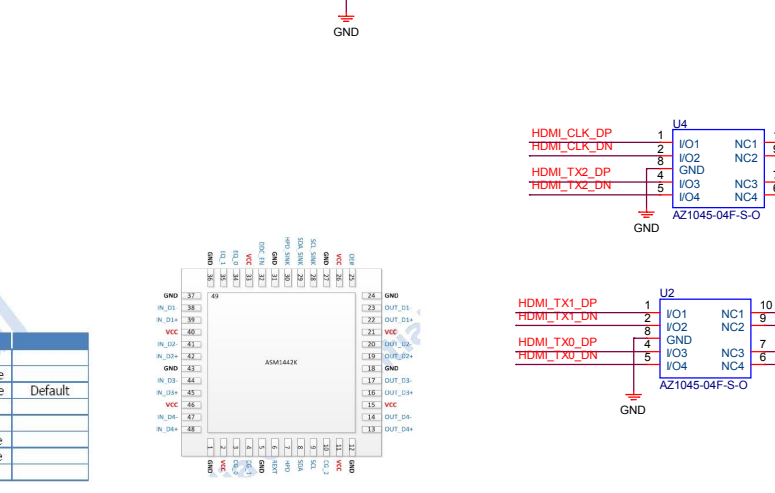
CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	



1/16 Amos: 11/11/16 solution

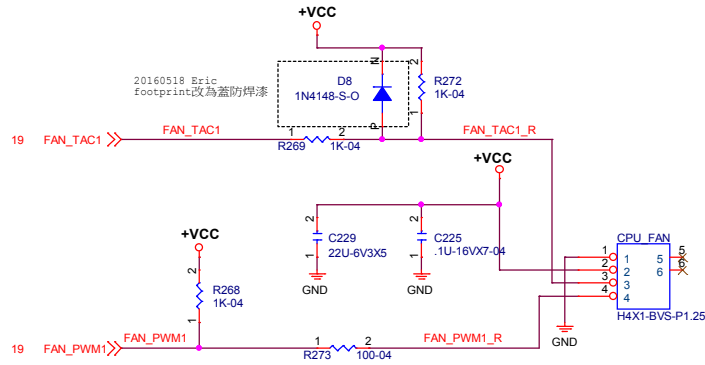


1/18 Amos: HDMI SI fail issue, follow 廠建議, 更改電阻成3.09K ASM1442K

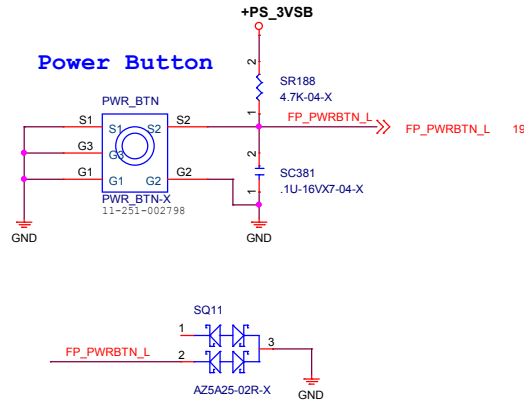




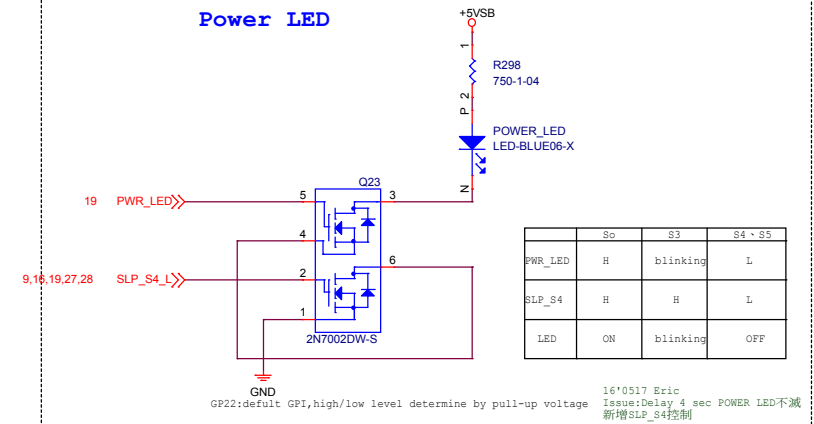
## FAN CONTROL header



## Power Button



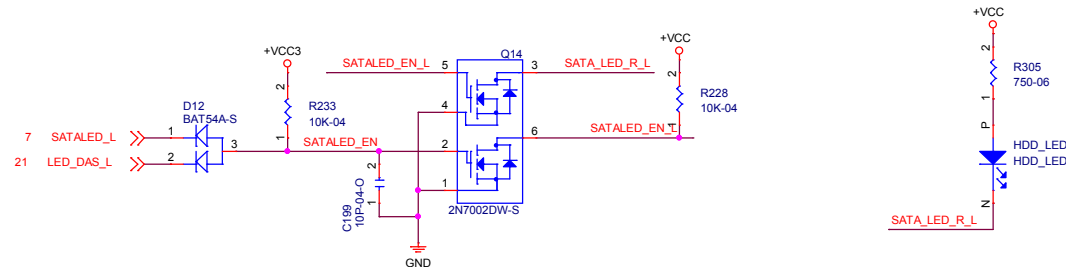
## Power LED



## 6. List of GPIO Pins

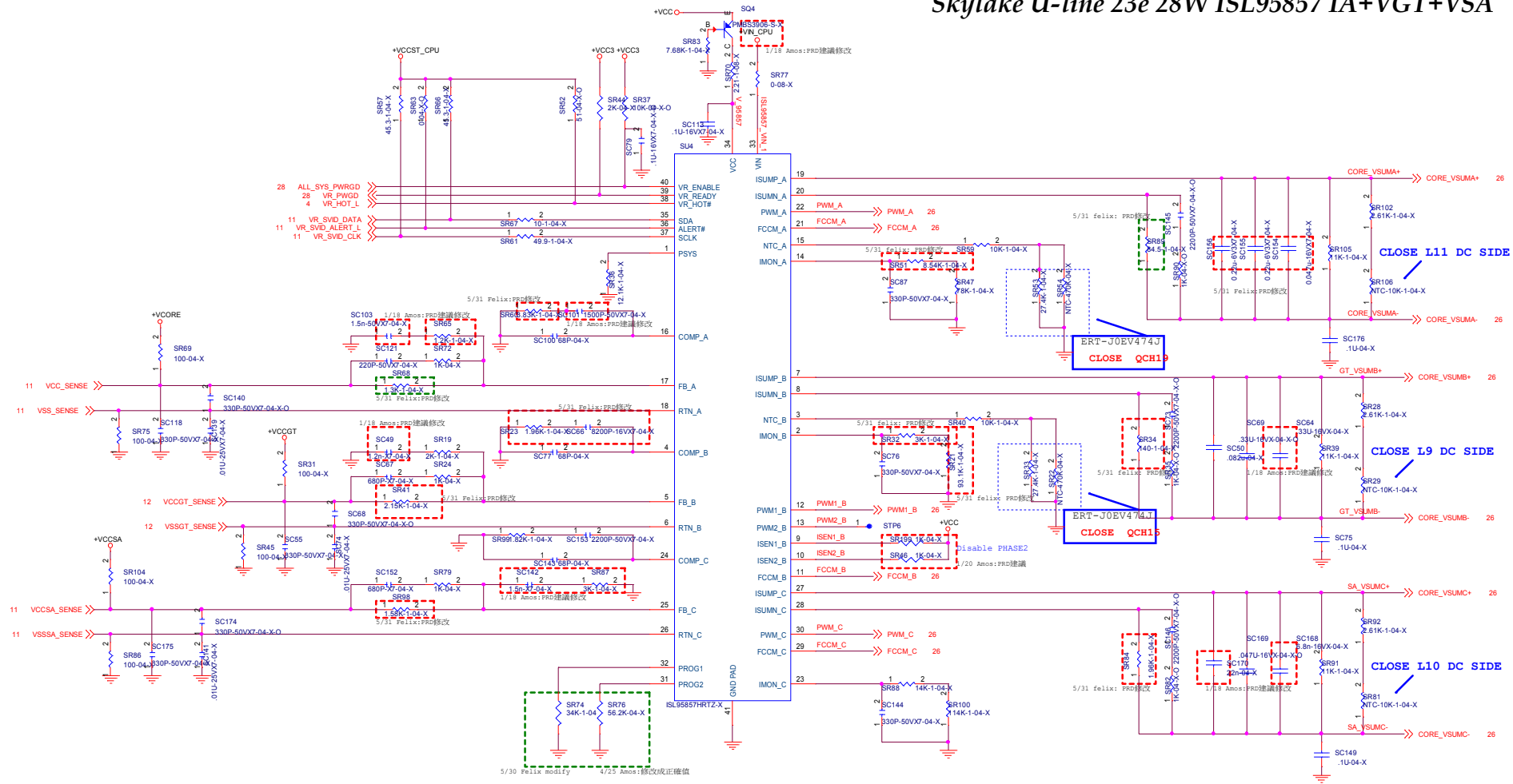
Table 6-1. GPIO Alternate Function

Group	Bit	Power By	Pin Loc.	1 <sup>st</sup> Func	Condition	2 <sup>nd</sup> Func	Condition	3 <sup>rd</sup> Func	Condition	4 <sup>th</sup> Func	Condition	Output Driving (mA)	Note
GPIO 1k	0	3VSB	40	PC10-DT0P (D10C40)		GPIO1K (D1)	250-0-0	GPIO1K (D10C40)	250-0-1			8mA	
	2	3VSB	11	PC10-DT0P (D10C40)		GPIO1K (D10C40)	250-0-1					8mA	
GP IO2K	0	3VSB	8	GPIO2K (D10C40)	250-0-1							8mA	
	2	3VSB	8	GPIO2K (D10C40)	250-0-1							8mA	





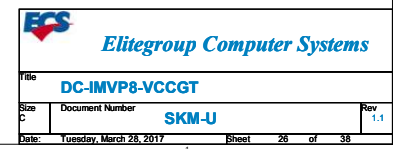
# Skylake U-line 23e 28W ISL95857 IA+VGT+VSA



Elitegroup Computer Systems

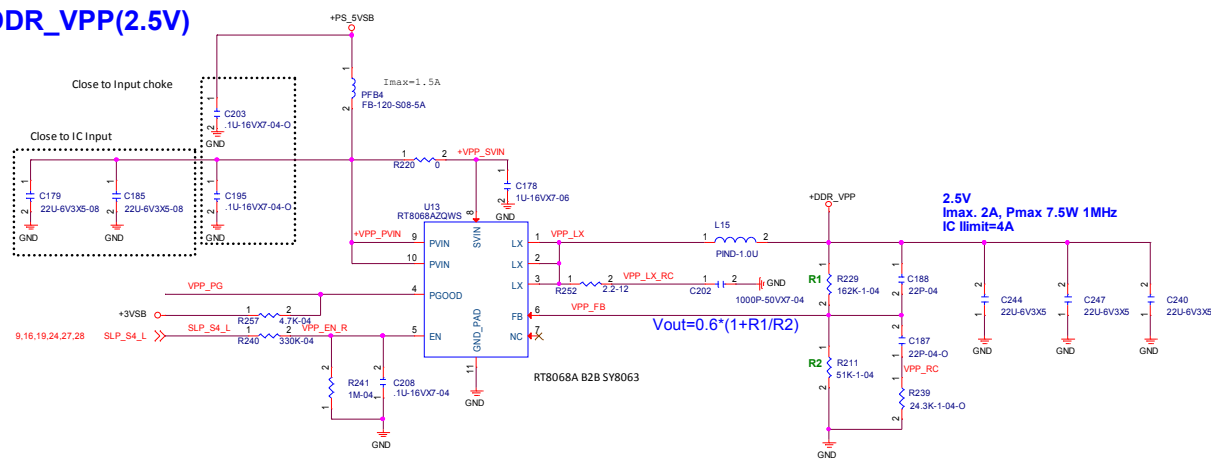
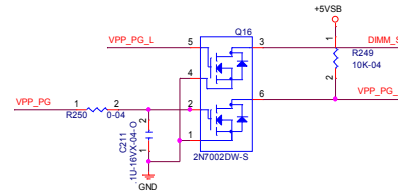
File	DC-IMVP8-VCORE		
Size	Document Number	SKM-U	Rev 1.1
Date	Tuesday, March 28, 2017	Sheet 25	of 38



[illegible]

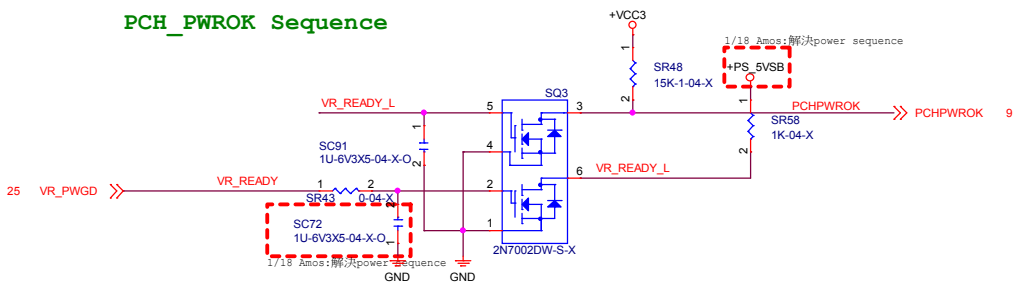


**+DDR\_VPP(2.5V)**

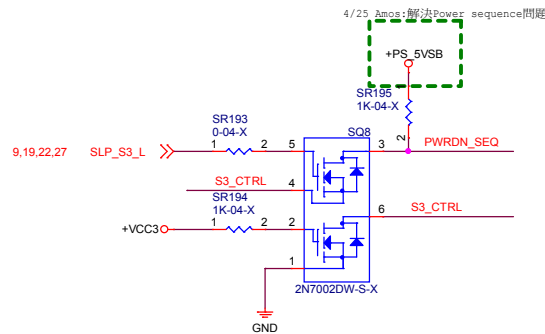
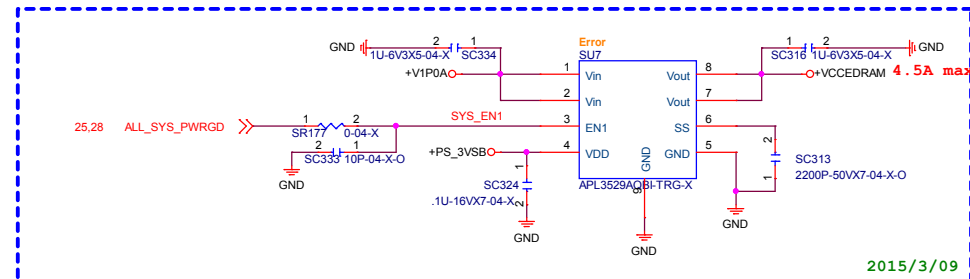
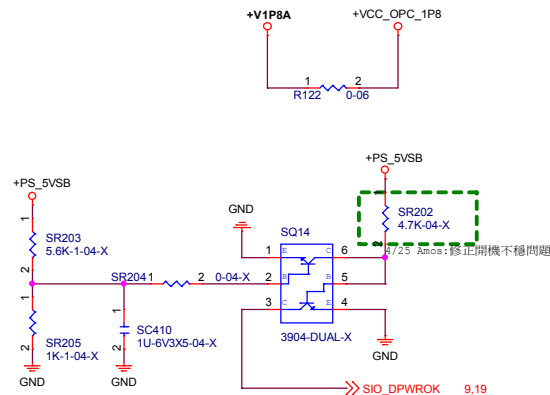
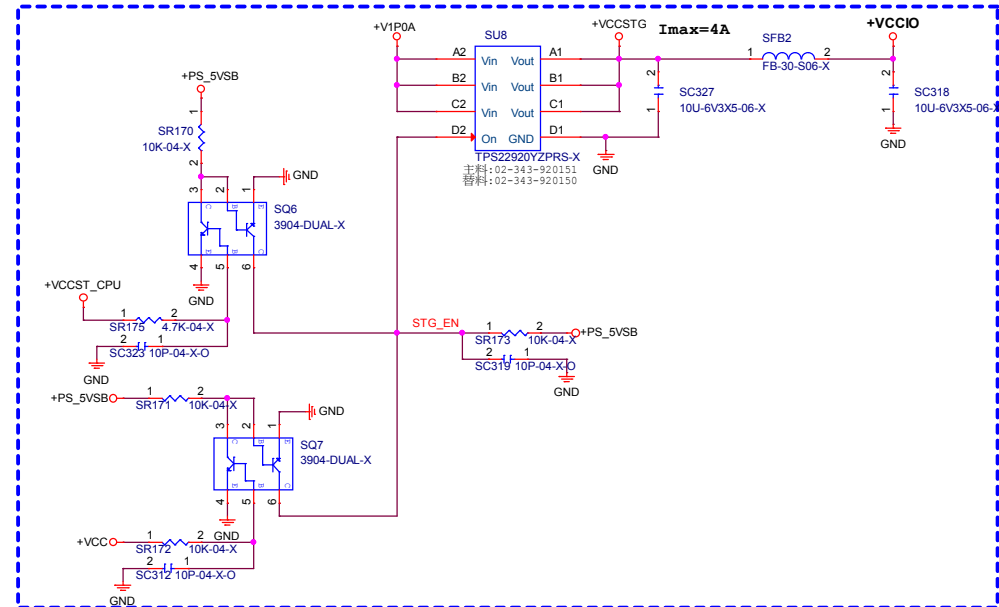
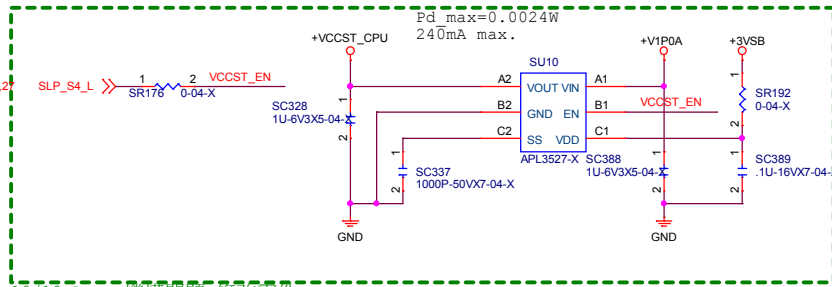
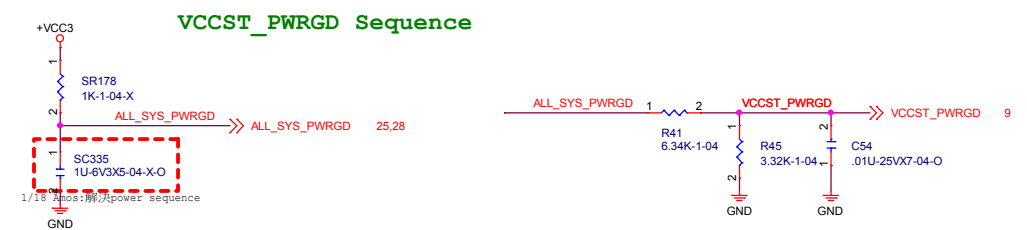




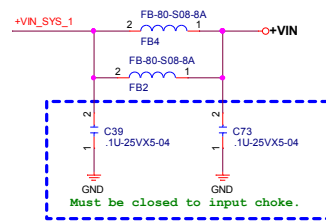
## PCH\_PWROK Sequence



## VCCST\_PWRGD Sequence

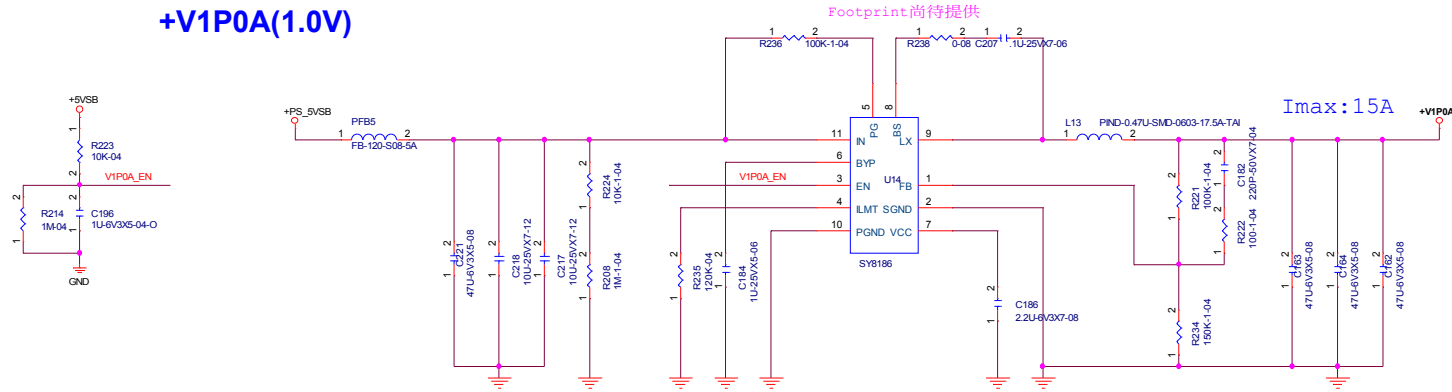






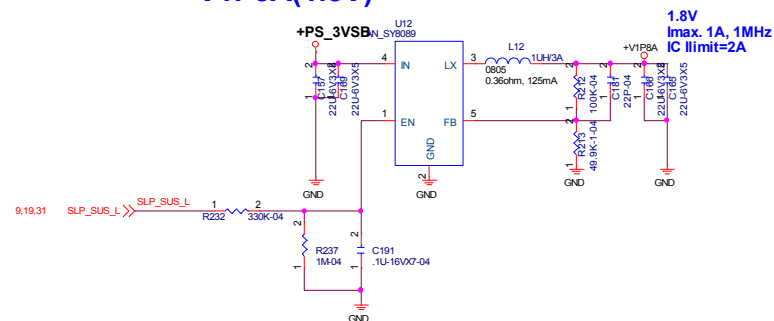


## +V1P0A(1.0V)



VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

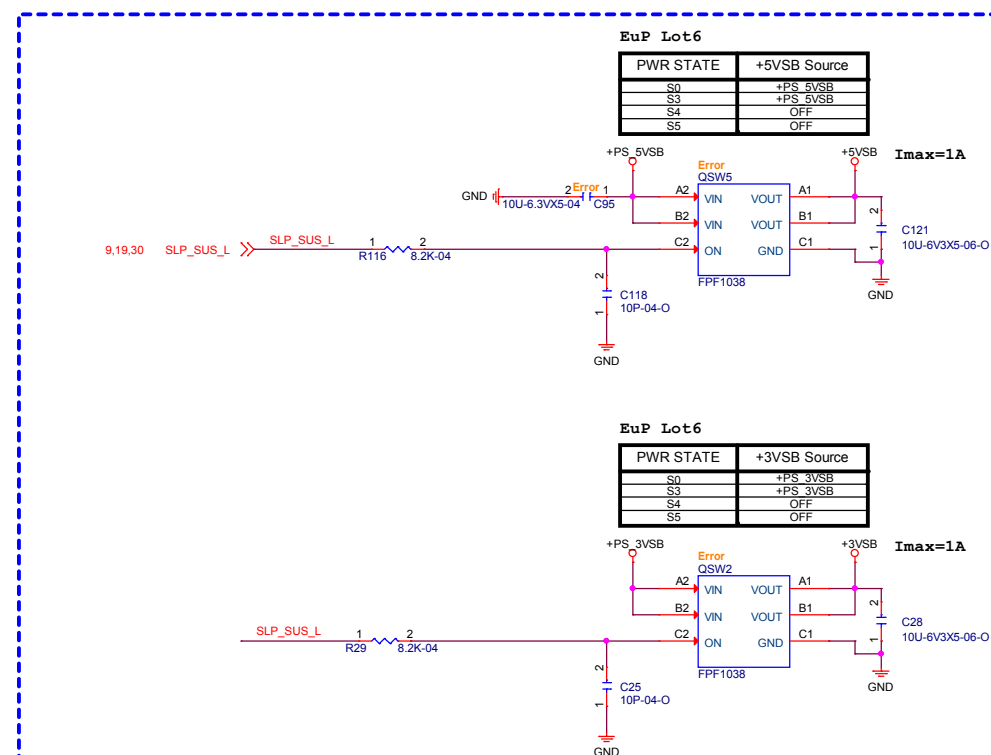
## +V1P8A(1.8V)



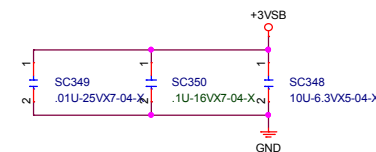
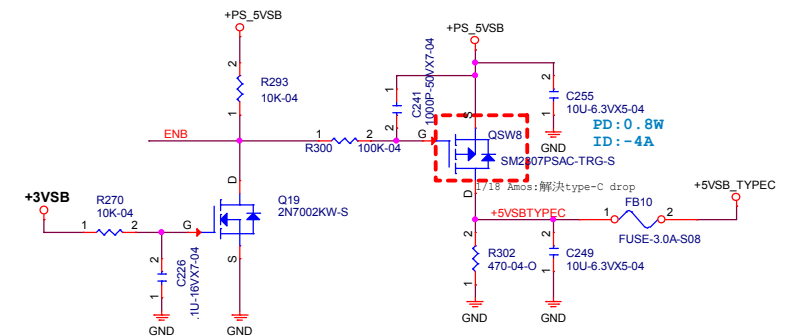
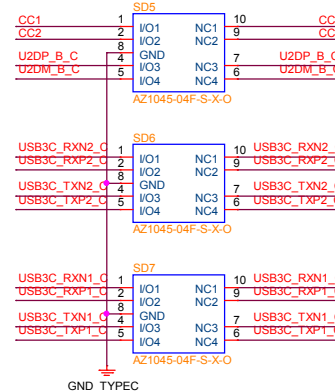
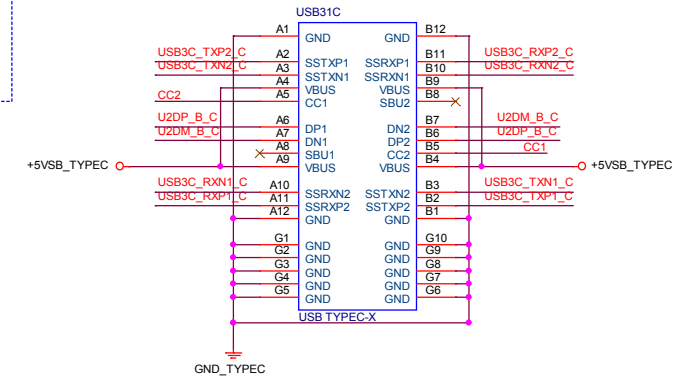
Elitegroup Computer Systems

Title			
+V1P0A/+V1P8A			
Size	Document Number	Rev	
Custom	SKM-U	1.1	
Date:	Tuesday, March 28, 2017	Sheet	30 of 38

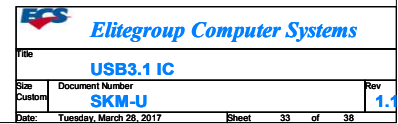






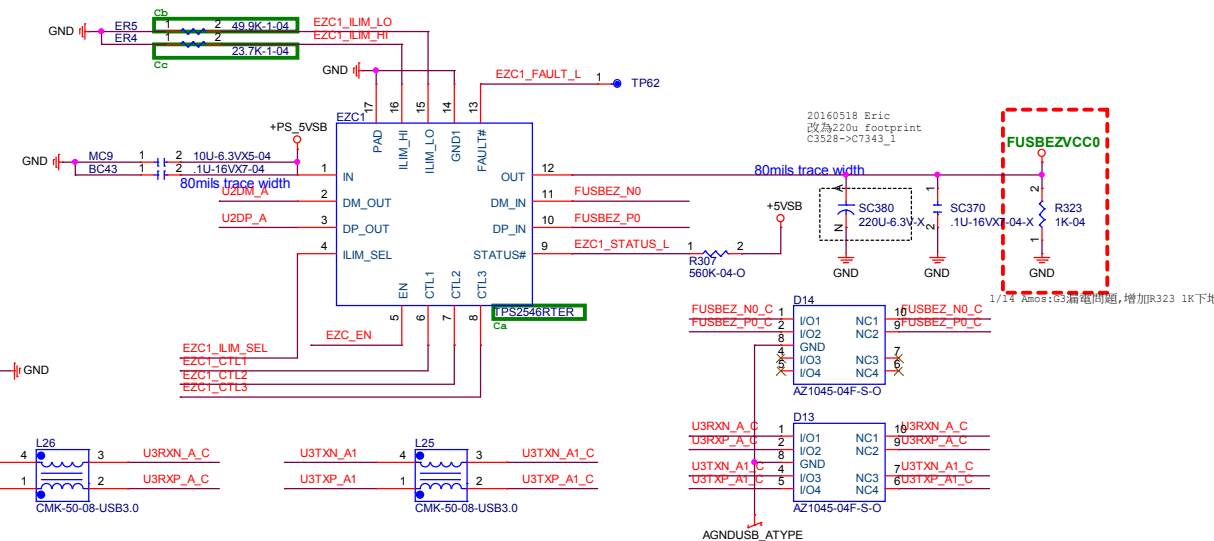






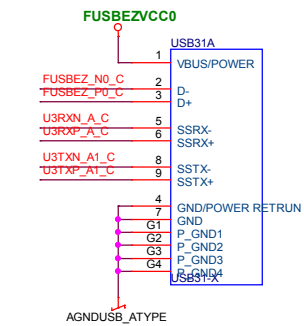


- 33 U3RXN\_A U3RXN\_A
- 33 U3RXP\_A U3RXP\_A
- 33 U3TXN\_A1 U3TXN\_A1
- 33 U3TXP\_A1 U3TXP\_A1
- 33 U2DP\_A U2DP\_A
- 33 U2DM\_A U2DM\_A
- 8 EZC1\_ILIM\_SEL EZC1\_ILIM\_SEL
- 8 EZC1\_CTL1 EZC1\_CTL1
- 8 EZC1\_CTL2 EZC1\_CTL2
- 8 EZC1\_CTL3 EZC1\_CTL3
- 4 EZC\_EN EZC\_EN



### CO-LAY BOM

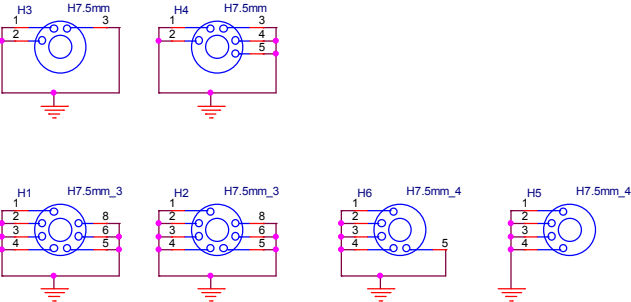
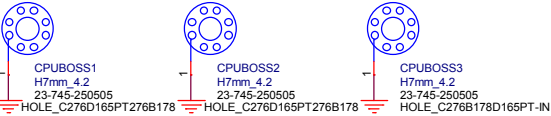
Ca	Cb	Cc
TPS2546RTER	49.9K-1-04	23.7K-1-04
VP200	33.2K-1-04	54.7K-1-04






PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	Top Swap Override	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default). for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap .
GSPI0_MOSI	No Reboot	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SMBALERT#	TLS Confidentiality	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GSPI1_MOSI	Boot BIOS Strap Bit BBS	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). 0 SPI (Default) 1 LPC
SML0ALERT#	eSPI or LPC	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA	Port B Detected	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected.
DDPC_CTRLDATA	Port C Detected	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected.





Elitegroup Computer Systems

Title104/STRAPPING		
Size Custom	Document NumberSKM-U	Rev1.1
Date: Tuesday, March 28, 2017	Sheet 35 of 38	



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status	Bios Set
GPP_B16	3VSB	GPP_B16(BIOS override)	GPI	GPO(Hi)
GPP_A18	3VSB	BIOS_CONFIG	GPI	GPI
GPP_A19	3VSB	GPP_A19(BIOS Config)	GPI	GPI
GPP_B20	DSW	PWR_LED	GPI	GPO(Hi)
GPP_B17	+V_3P3_LAN	WLAN_DISABLE_L	GPI	GPO(Hi)
GPP_C8	3VSB	USB_charger EN	GPI	GPO(Hi)
GPP_C21	VCC3	LOGO_LED	GPI	GPO(Low)
GPP_C22	VCC3	USB3.1 SMI	GPI	SMI(follow Z170-claymore)
GPP_C23	3VSB	USB3.1 WAKE	GPI	GPI
GPP_C18	+V_3P3_LAN	M.2 ALERT	GPI	GPI
GPP_B3	+V_3P3_LAN	BT_DISABLE	GPI	GPO
GPP_D9	VCC3	HDMI_ENABLE	GPI	GPO(Low)
GPP_D19	3VSB	ILM_SEL	GPI	GPO(follow Z170-claymore)
GPP_D20	3VSB	CTL1	GPI	GPO(follow Z170-claymore)
GPP_D17	3VSB	CTL2	GPI	GPO(follow Z170-claymore)
GPP_D18	3VSB	CTL3	GPI	GPO(follow Z170-claymore)
GPP_D2	VCC3	BOM select	GPI	GPI
GPP_D3	VCC3	BOM select	GPI	GPI
GPP_D0	VCC3	BOM select	GPI	GPI
GPP_D21	VCC3	BOM select	GPI	GPI
GPP_D22	VCC3	BOM select	GPI	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP22	PS_5VSB	PWR_LED(S0=>low , S3=>blinking)	

PCH-INT Function

Function	INT Port	PCIE_X1 Port	Device
LAN Ethernet Controller	INT B#	PE_TX/RX_4	LAN-I219V
AC-8260(M.2)_WLAN	INT A#	PE_TX/RX_5	AC_8260
PCIE_M.2(22x80)	INT A#	PE_TX/RX_9	PCIE_M.2
SATA Controller	INT C#	N/A	SATA



# PWR Sequence & RST Diagram

